

PWA :
PWB : Y509R
SCH : Y510R

Calpella Intel Discrete Block Diagram

VER :C2A

POWER

AC/BATT CONNECTOR	PG 55
BATT CHARGER	PG 45

CLOCK SLG8SP585V (QFN-64)	PG 15
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FAN & THERMAL EMC1422 (8P TSSOP)	PG 37
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Clarksfield (Qual Core)

SYSTEM POWER

PCH REGULATOR +1.05V_PCH PG 49	SYS VR +5V_ALW2/+3.3V_ALW +5V_ALW/+15V_ALW PG 51	VGA Core +VCC_GFX_CORE +1.1V_GFX_PCIE PG 52
DDR3 VR +1.5V_SUS/+0.75V_DDR_VTT PG 47	CPU VR +1.1V_VTT PG 48	REGULATOR +1.8V_RUN PG 46
Load Switch +5V_SUS/+3.3V_SUS/+5V_RUN/ +3.3V_RUN/+1.5V_RUN/ +1.5V_GDDR PG 54	VCC Core +VCC_CORE PG 50	VGA VDDCI +VDDCI PG 53

DDR3-SODIMM1	PG 13	800 / 1066 MHZ DDR III
DDR3-SODIMM2	PG 14	800 / 1066 MHZ DDR III

Subwoofer CONN	PG 40
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Subwoofer AMP MAXIM MAX9759 (16 Pin TQFN)	PG 40
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AUDIO IDT 92HD73C (56 LQFP) 9 x 9 mm	PG 38
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MIC
Internal Speaker

Amplifier TI TPA6040A4 (32 Pin QFN)	PG 39
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HP2
HP1

Amplifier TI TPA4411MRTJR (20 Pin QFN)	PG 39
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Camera + D-MIC	PG 35
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TV CONN	PG 33
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USB CONN

USB/eSATA Combo PG 33 & eSATA board
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SATA-ODD	PG 34
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SATA-HDD	PG 34
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1394 CONN	PG 27
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CardReader CONN	PG 27
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PC Card/1394 RICOH R5U230 (48 Pin QFN) 6 x 6 mm	PG 26
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Ibex Peak-M

SIO ITE ITE8512E (128 Pin LQFP) 16 x 16 mm	PG 29
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SPI ROM 2MB (8 Pin SO8W)	PG 30
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Keyboard	PG 35
----------	-------

CIR	PG 30
-----	-------

Touchpad

Media Button

LED	PG 36
-----	-------

RTC	PG 30
-----	-------

AMD Madison XT PCI EXPRESS GFX (962 FCBGA)	PG 17,18,19,20
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DDR3 x 8 (1G, 64Mx16 bit) (100P FBGA)	PG 21,22
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WWAN MINI-CARD	PG 32
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WLAN Half MINI-CARD	PG 31
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UWB/BT MINI-CARD	PG 32
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Express Card	PG 28
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LAN Broadcom BCM5784M (68P QFN)	PG 41
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PAD & SCREW & SPRING	PG 44
----------------------------	-------

System Reset Circuit	PG 43
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To IO Board (USB*2/ MIC/ HP2/ HP1/ LED)	PG 40
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To Daughter Board (Power Button/Speaker/ KB LED/Touch PAD/ Media Button)	PG 35
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HDMI	HDMI CONN.	PG 23
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DP	DISPLAYPORT	PG 23
----	-------------	-------

LVDS	Panel Connector	PG 24
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VGA	CRT CONN.	PG 25
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GPU THERMAL ANALOG DEVICES ADM1032 (8 MSOP) 3 x 3 mm	PG 20
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Express Switch RICOH R5538D001 (20 QFN) 4 x 4 mm	PG 28
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Magnetic	PG 42
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RJ45	PG 42
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
Title	BLOCK DIAGRAM
Size	Document Number Calpella
Date	Tuesday, November 10, 2009
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Rev	C2A

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25	CRT
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27	Card reader & 1394 CONN
28	Express card
29	SIO (IT8512)
30	Flash/RTC/CIR
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32	WWAN/WPAN
33	USB & eSATA & TV
34	SATA HDD & ODD
35	KB/CCD/UI
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37	FAN/Thermal
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45	CHARGER (MAX8731A)
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49	1.05V_PCH (TPS51218)
50	VCC_CORE(MAX17036GTL+)
51	3.3V/5V/15V (MAX17020)
52	VGA_M97(MAX8792)
53	VDDCI_M97(TPS51218)
54	Run Power Switch
55	DCIN & Batt
56	XDP Connector
57	Power Block Diagram
58	SMBUS BLOCK
59	Power status

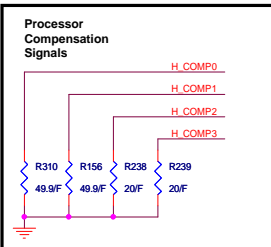
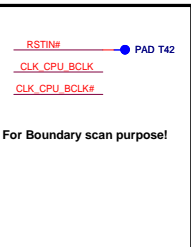
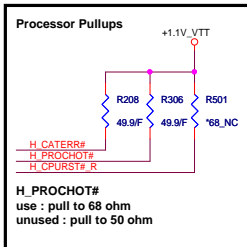
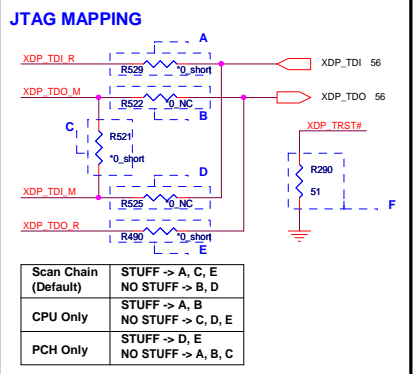
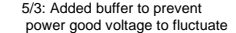
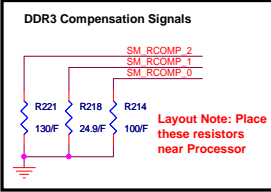
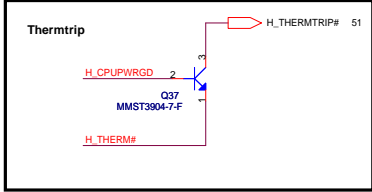
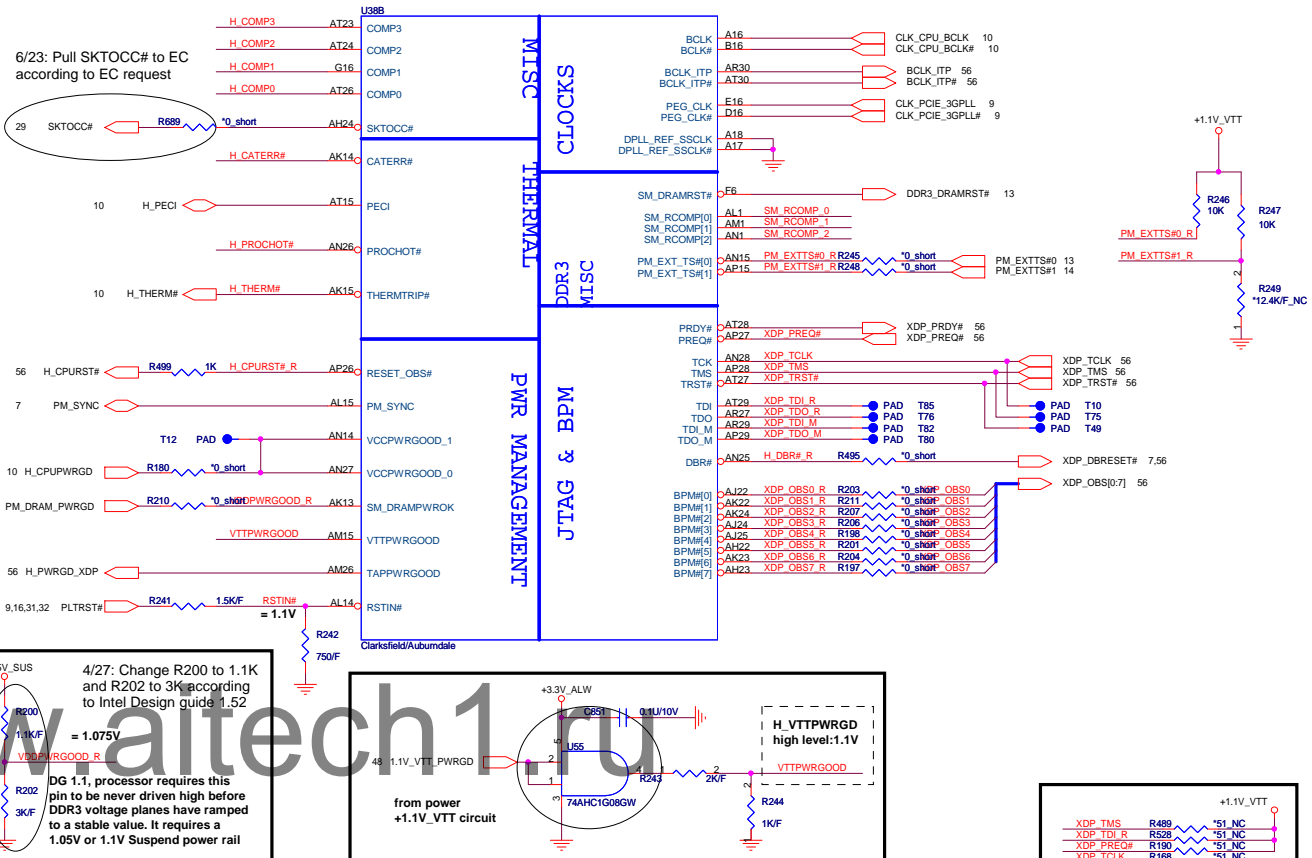
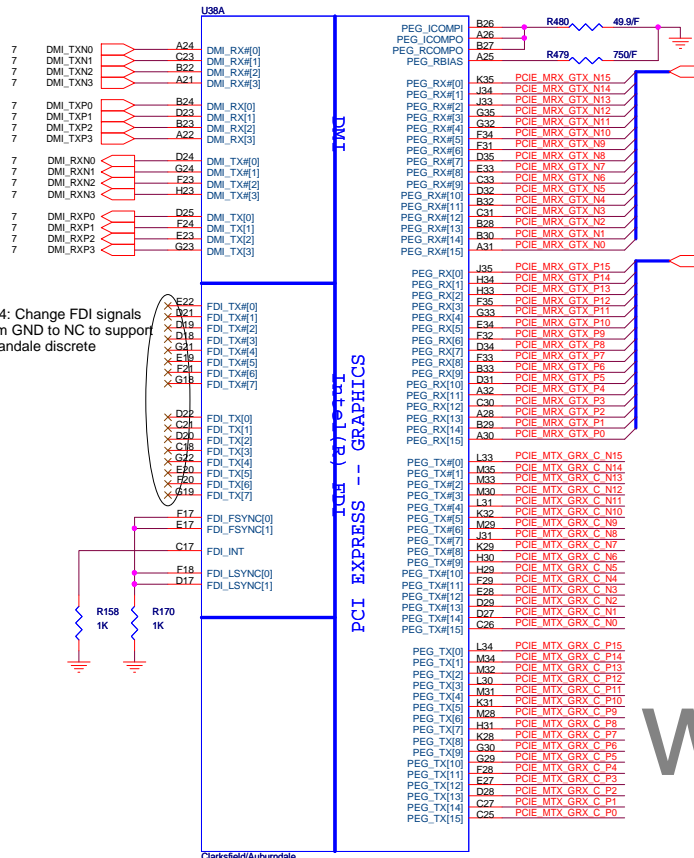
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51,52,53	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	8,11,29,30	RTC		S0~S5
+3.3V_ALW	+3.3V	3,29,30,34,35,36,43,45,51,54,55	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	24,33,34,35,47,51,52,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	24,34,51,54	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	41,42	LAN POWER	AUX_ON	
+5V_SUS	+5V	11,46,48,49,52,53,54	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	7,8,9,10,11,20,24,28,29,42,43,46,47,48,49,52,53,54	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.5V_SUS	+1.5V	3,5,13,14,47,52,54	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,54	SODIMM POWER	SUS_ON	
+5V_RUN	+5V	11,18,23,25,33,35,36,37,38,50,54	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	7,8,9,10,11,13,14,15,18,23,24,26,28,29,30,31,32,33,34,35,36,37,38,39,40,41,50,52,54,56	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	5,11,17,18,19,46,54	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	28,31,32,54	PCH POWER	1.5V_RUN_ON	
+1.1V_VTT	+1.1V	3,5,10,11,48,50,56	CPU POWER	RUN_ON	
+1.05V_PCH	+1.05V	8,9,11,15,49	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.5V	5,50	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	34	Module Power	MODC_EN#	
+5V_HDD	+5V	34	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	35,36,51,54,55	LED power source	LDO output	

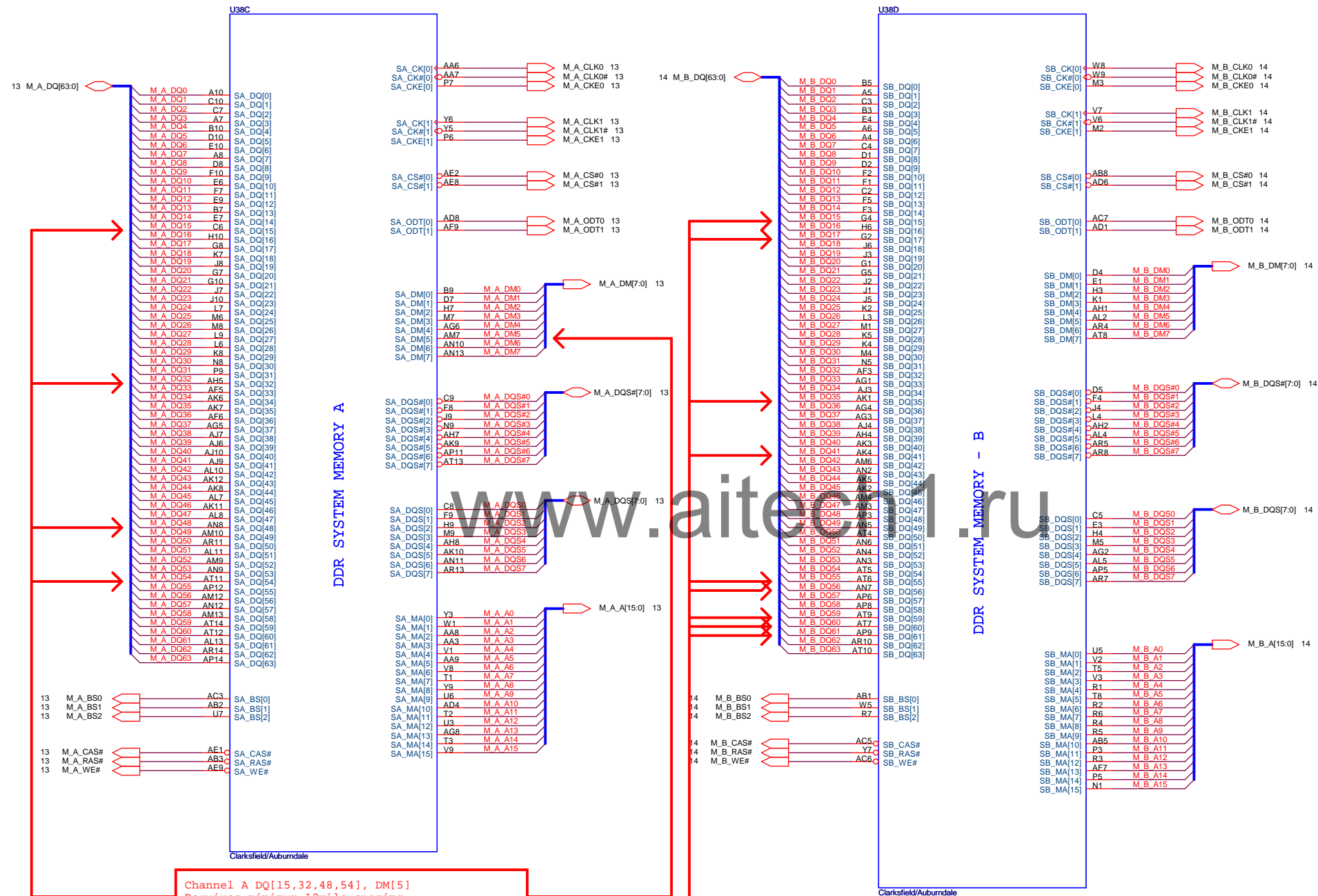
GND PLANE	PAGE	DESCRIPTION
 AGND	38,39,40	
 AGND_DC/DC	51	
 AGND_VCORE	50	
 GND	ALL	

AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

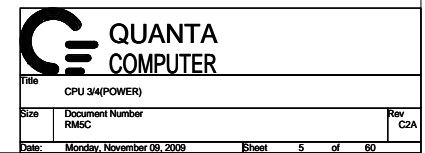
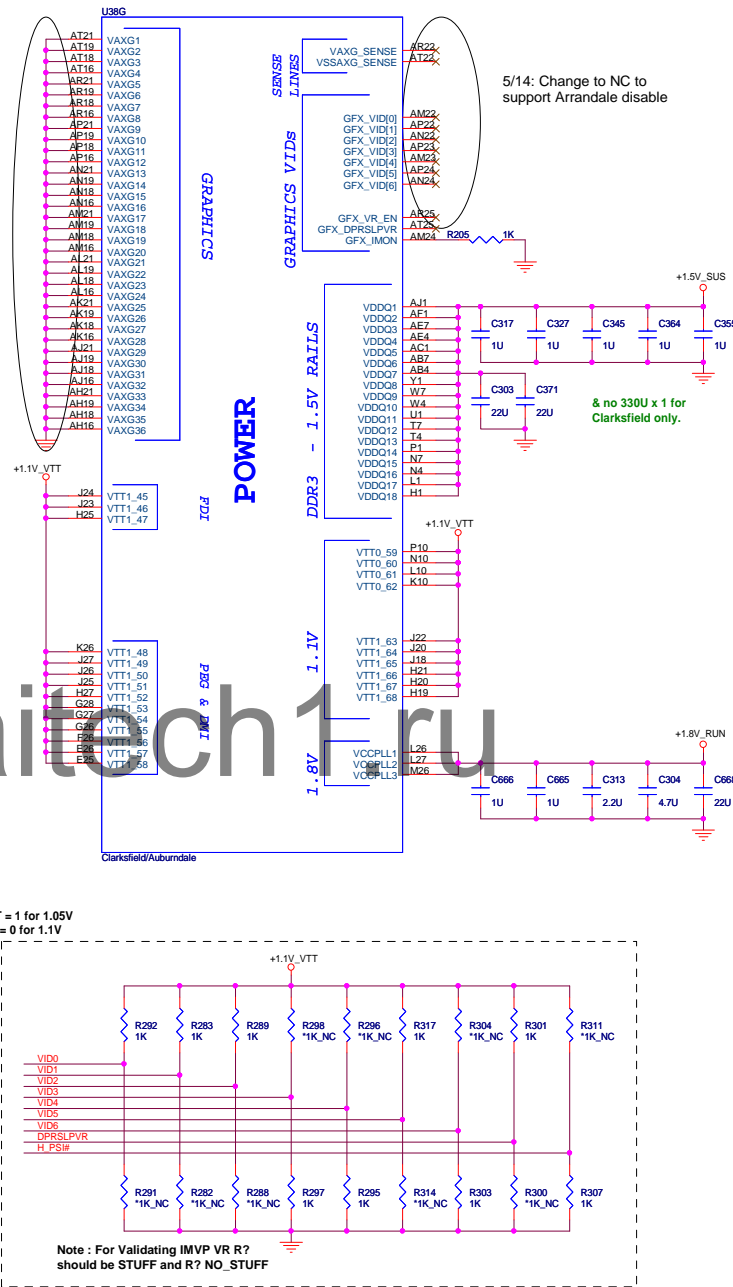


AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



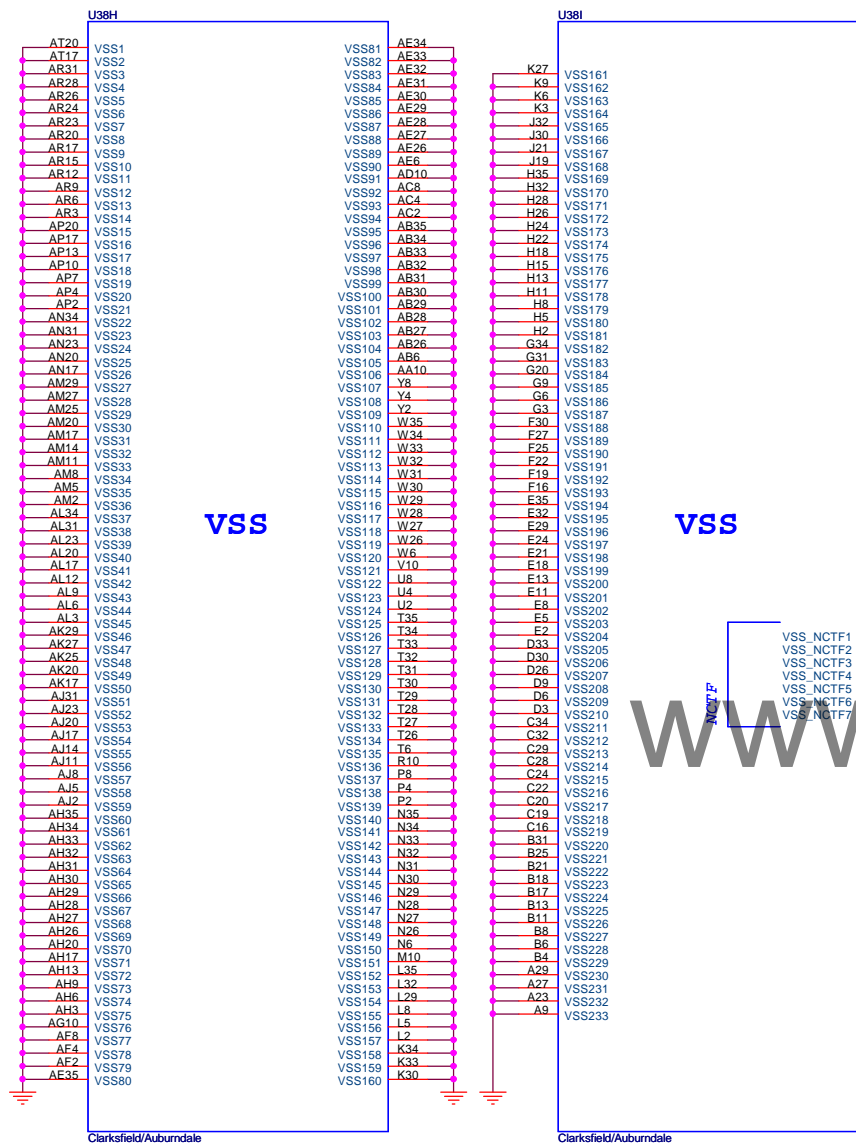
Title			
CPU 2/4(DDR)			
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AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

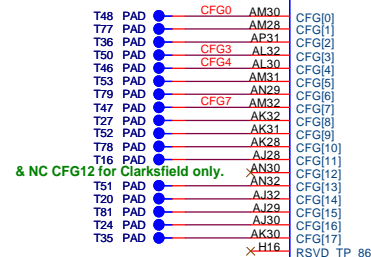


AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

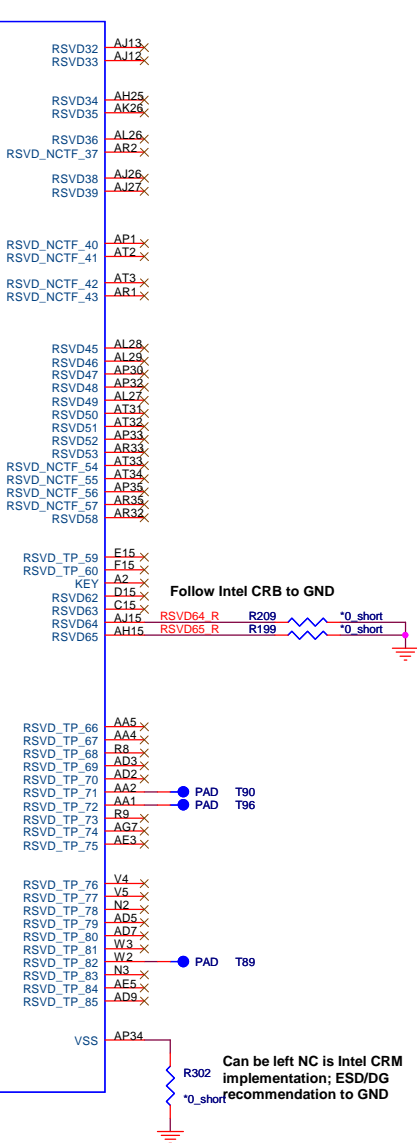
AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Generated
SO-DIMM VREF_DQ (M3)
Connect to page 13, 14

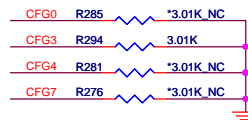


RESERVED



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Scott_0630:Change R294
footprint from RC0402-C to
RC0402



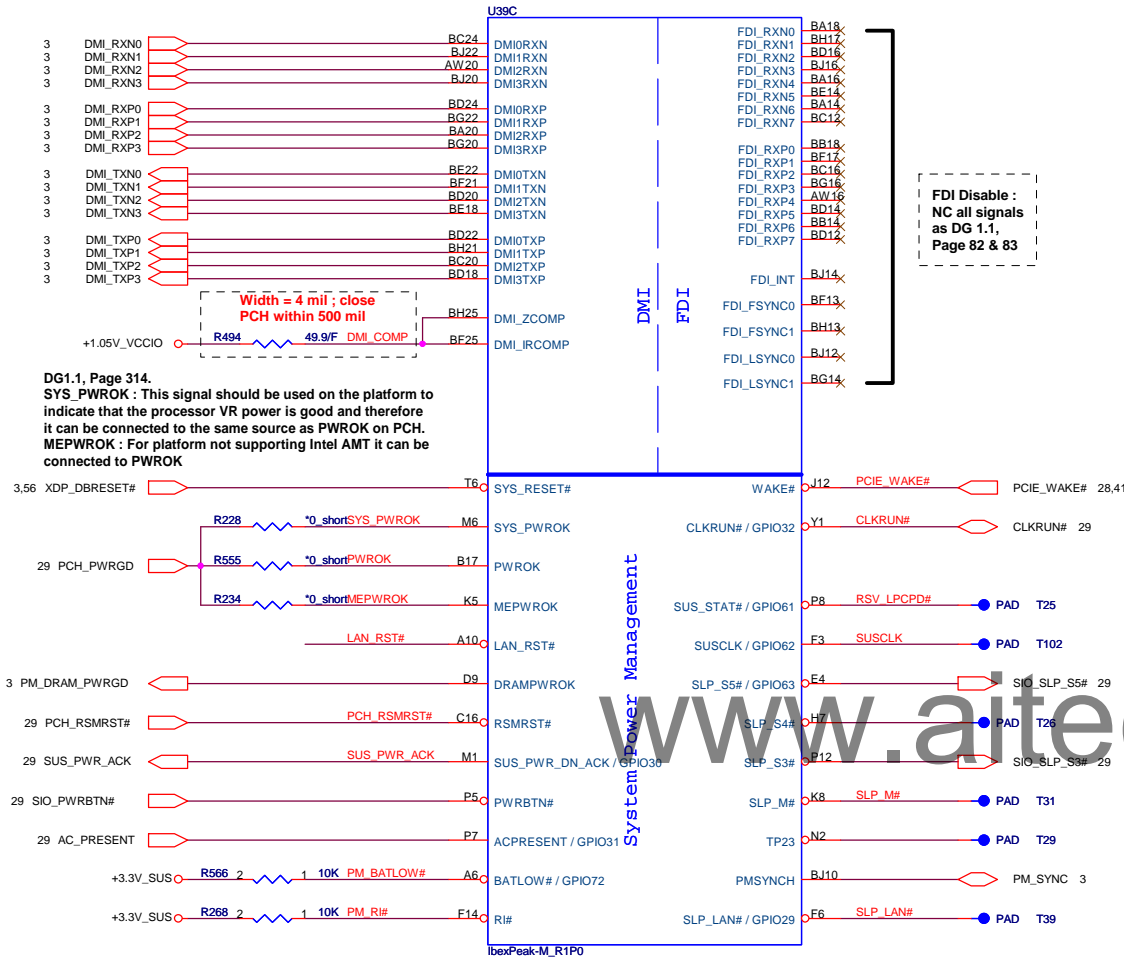
The Clarkfield processor's PCI
Express interface may not meet
PCI Express 2.0 jitter
specifications. Intel recommends
placing a 3.01K +/- 5% pull down
resistor to VSS on CFG[7] pin for
both rPGA and BGA components.
This pull down resistor should be
removed when this issue is fixed.

	1	0
CFG0 (PCI-Epress Configuration Select)	Single PEG (Default)	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation (Default)	Lane Numbers Reversed
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port (Default)	Enabled; An external Display port device is connected to the Embedded Display port
CFG7 Clarkfield (only for early samples pre-ES1)	Common motherboard design	For early samples pre-ES1 CFD (Default)



Title CPU 4/4(GND_RESV)		
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IBEX PEAK-M (DMI,FDI,GPIO)

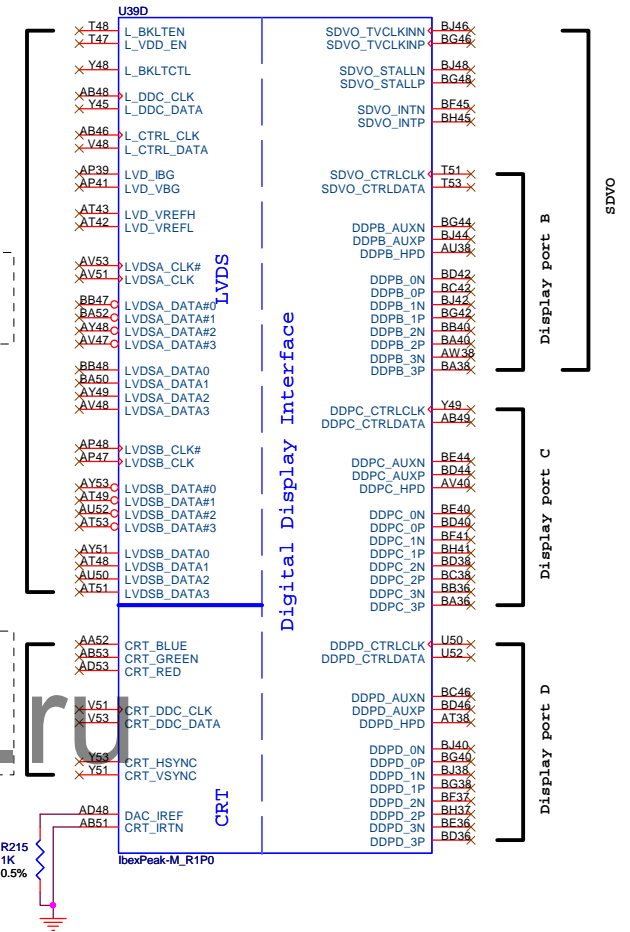


FDI Disable :
 NC all signals as DG 1.1, Page 82 & 83

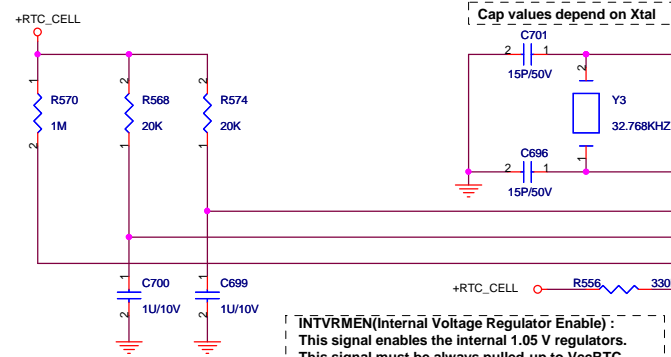
LVDS Disable :
 All signals associated with the interface can be left as No connects.

CRT Disable :
 CRT_RED
 CRT_GREEN
 CRT_BLUE
 CRT_HSYNC
 CRT_VSYNC
 Leave as NC (floating).

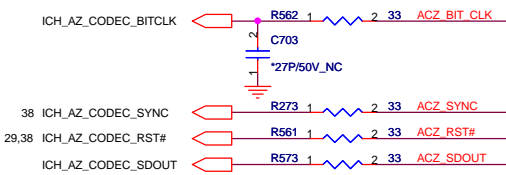
IBEX PEAK-M (LVDS,DDI)



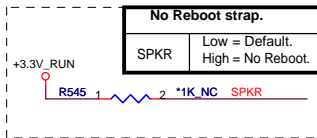
IBEX PEAK-M (HDA,JTAG,SATA)



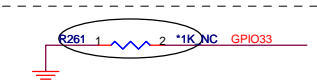
INTVRMEN (Internal Voltage Regulator Enable) :
This signal enables the internal 1.05 V regulators.
This signal must be always pulled-up to VccRTC.



Place all series terms close to PCH (within 500 mil) except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

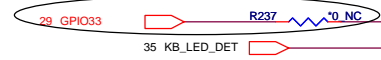


Scott_0630:Change R545 footprint from RC0402-C to RC0402.

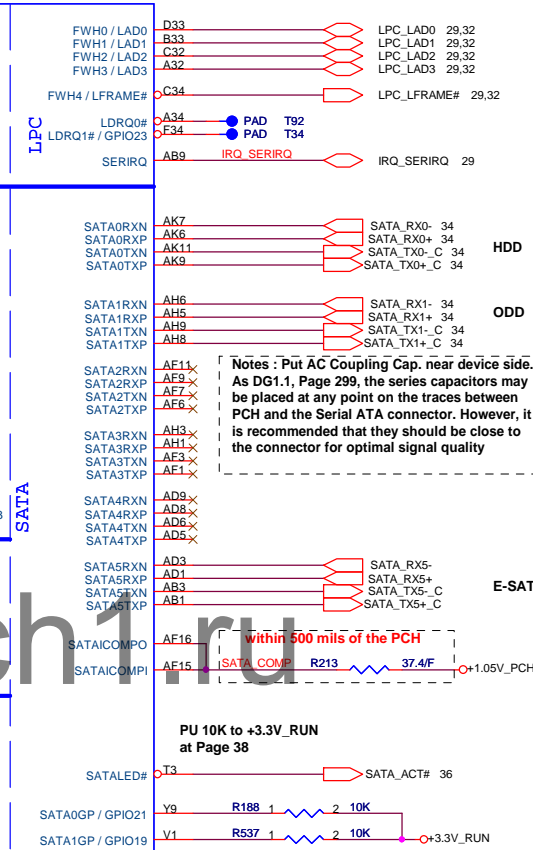
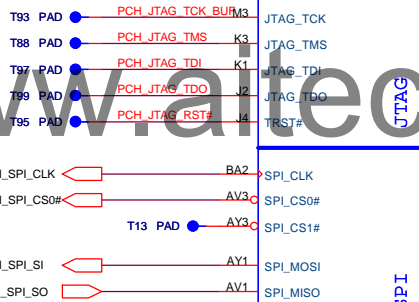


Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.

6/2: Change R261 from 10K_NC
to 1K_NC according to Intel design guide 1.51



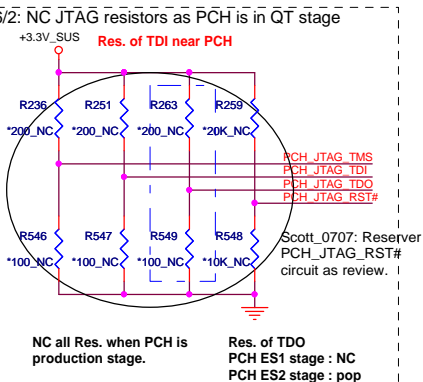
1007 for change list



Notes : Put AC Coupling Cap. near device side.
As DG1.1, Page 299, the series capacitors may be placed at any point on the traces between PCH and the Serial ATA connector. However, it is recommended that they should be close to the connector for optimal signal quality

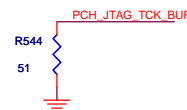
Notes : FIS-based Port Multiplier support on SATA Ports 4 and 5 in AHCI/RAID mode.

PU 10K to +3.3V_RUN
at Page 38



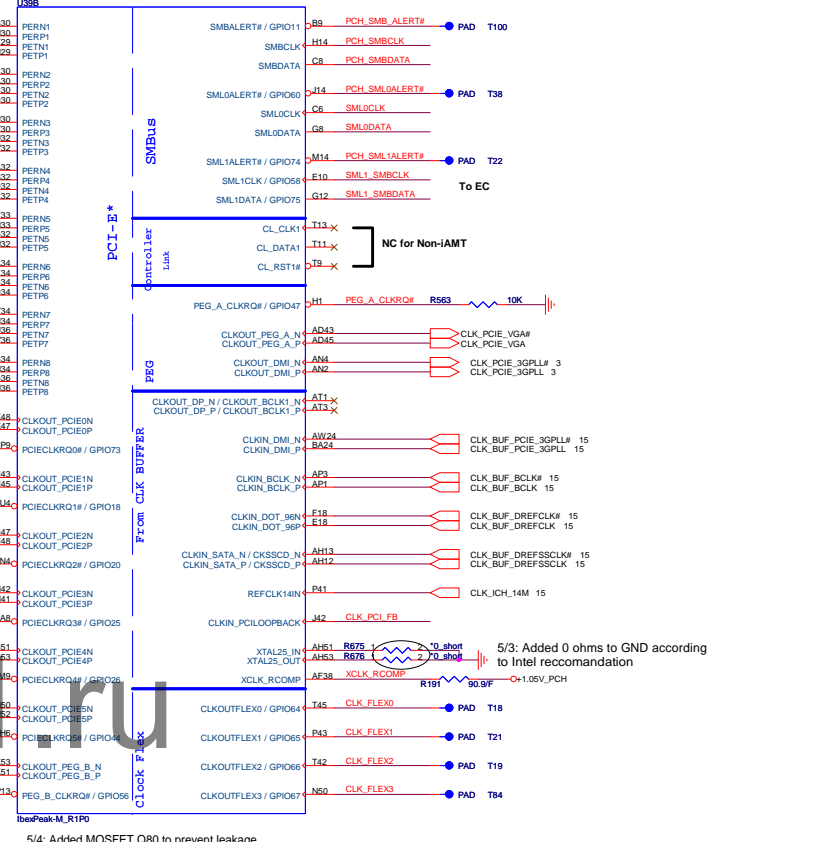
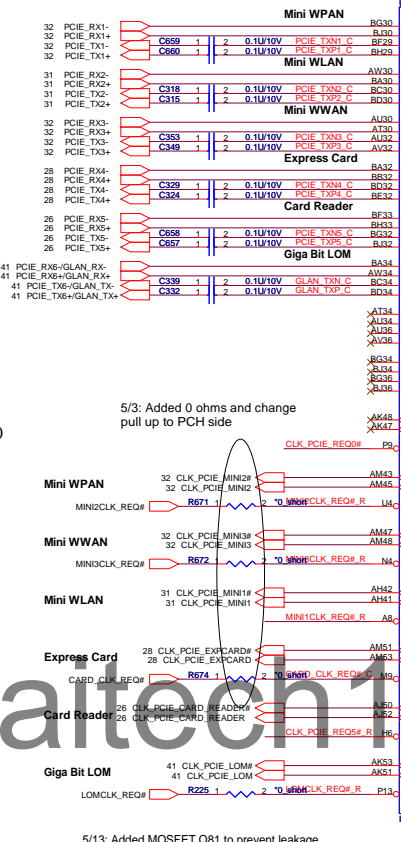
Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

Scott_0703 : Note : Delete pull up 1.05V according to Intel change notice! (Reserved for debug purpose)

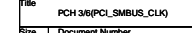
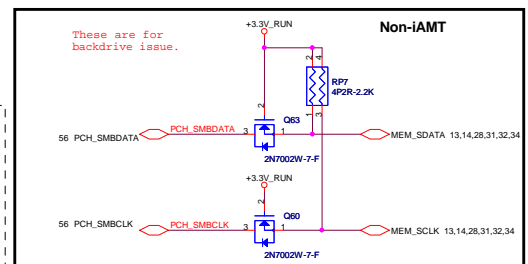
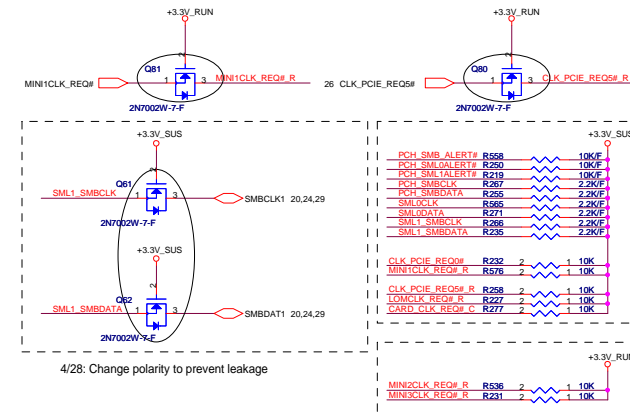


Title			
PCH 2/6(SATA_SPI)			
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IBEX PEAK-M (PCI-E,SMBUS,CLK)

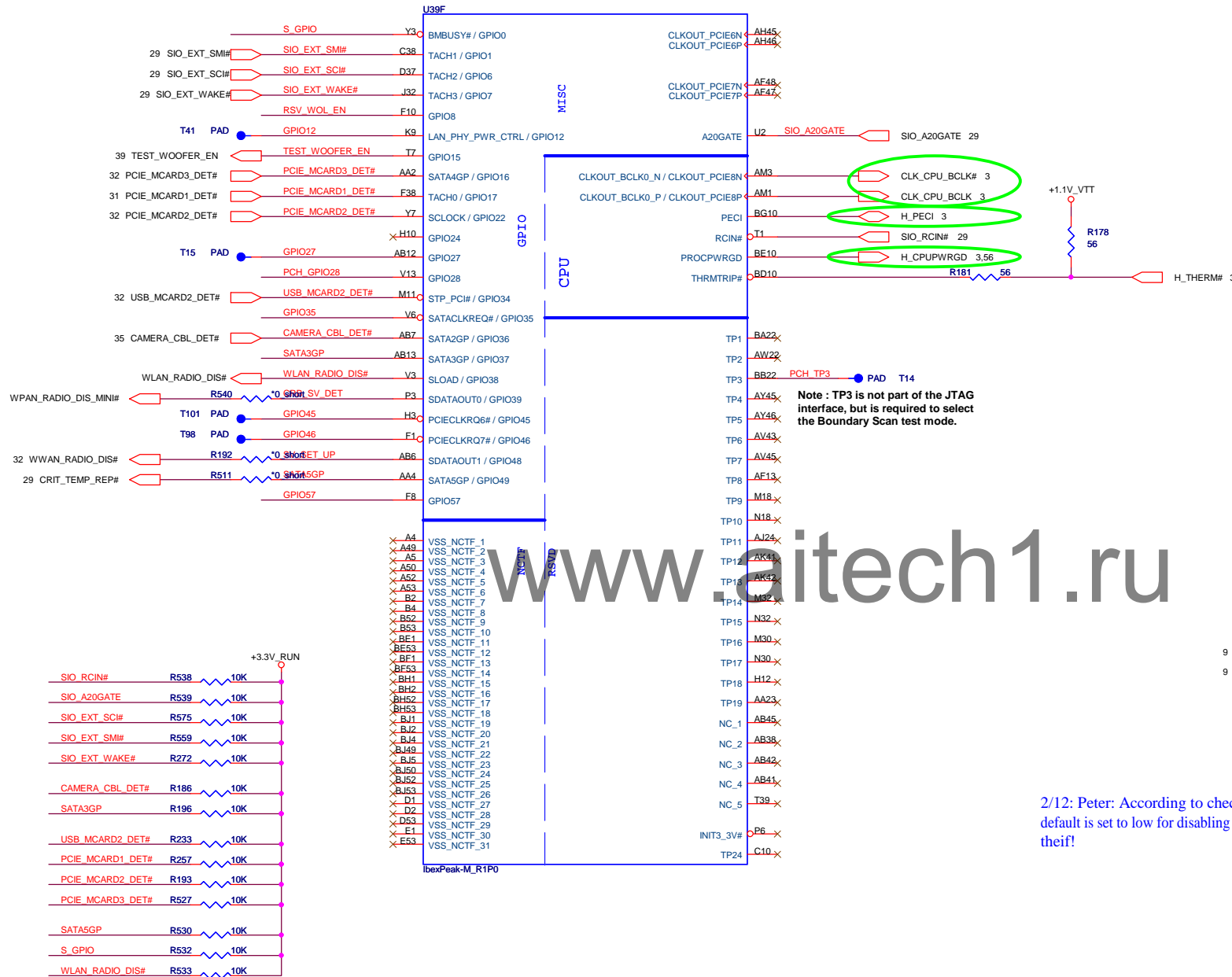


5/4: Added MOSFET Q80 to prevent leakage from 3.3V SUS to cardreader during S3

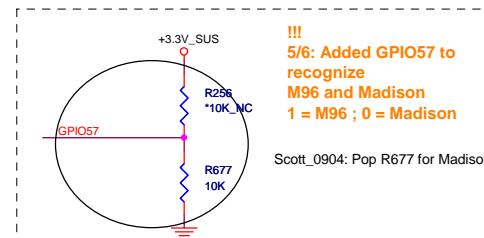
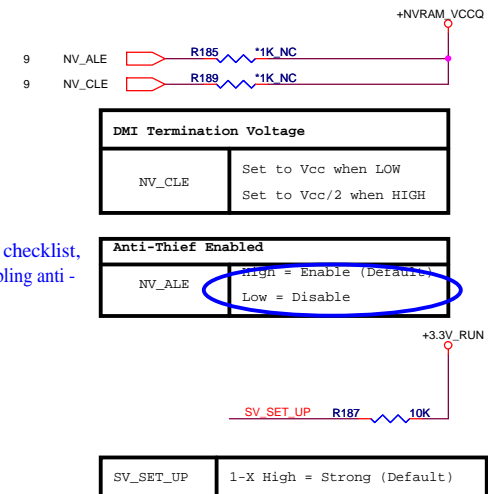


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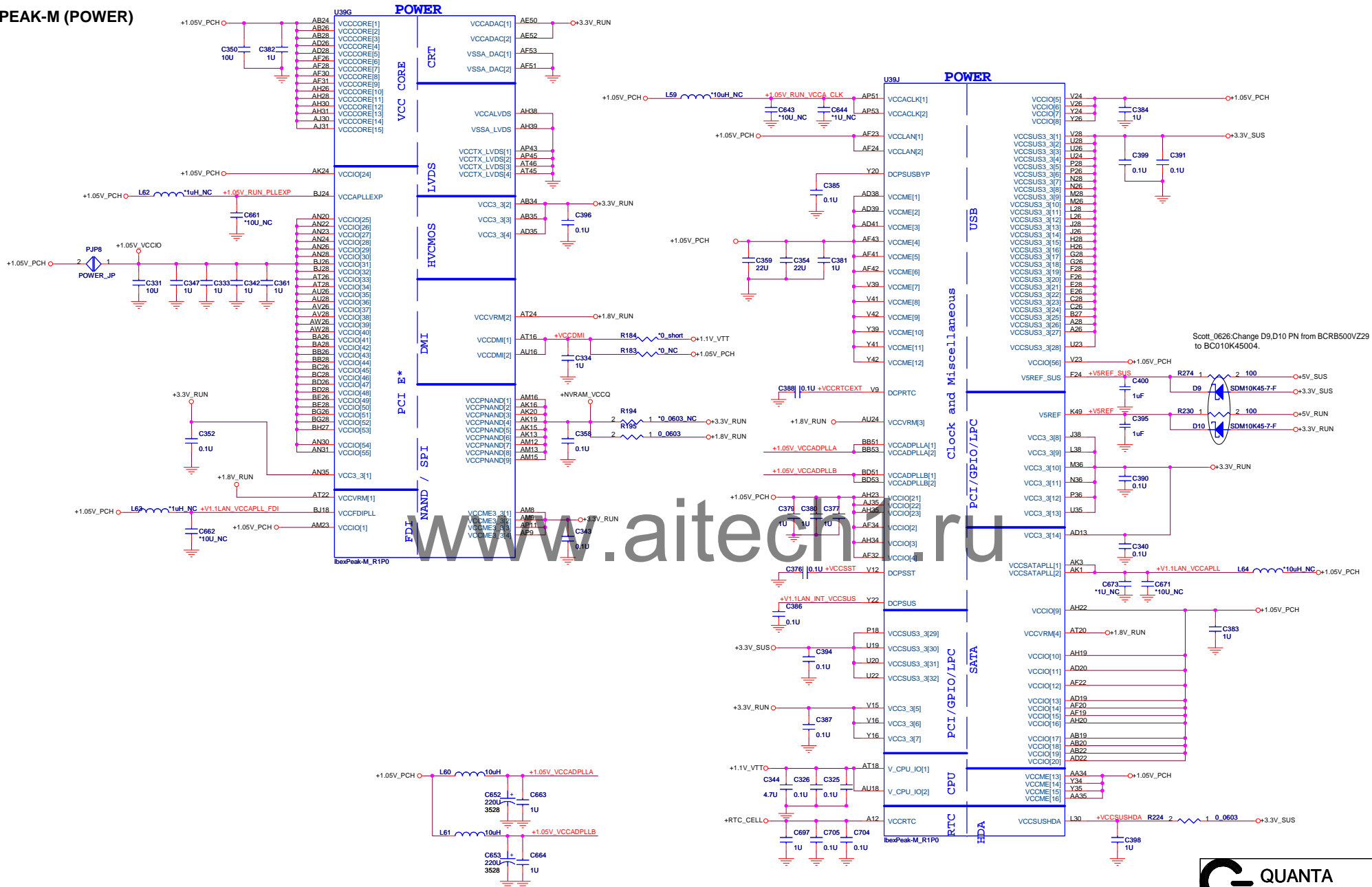
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



2/12: Peter: According to checklist, default is set to low for disabling anti-theft!



IBEX PEAK-M (POWER)



Use External Graphics. Can connect power directly without Inductor & Cap ? As Ibex peak-M EDS 1.0, need +1.05V. Can use +1.1V_VTT as CPU ?



Title PCH 5/6(POWER)

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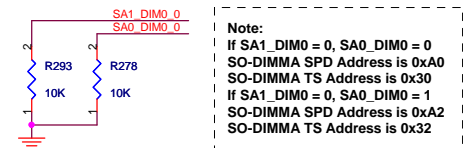
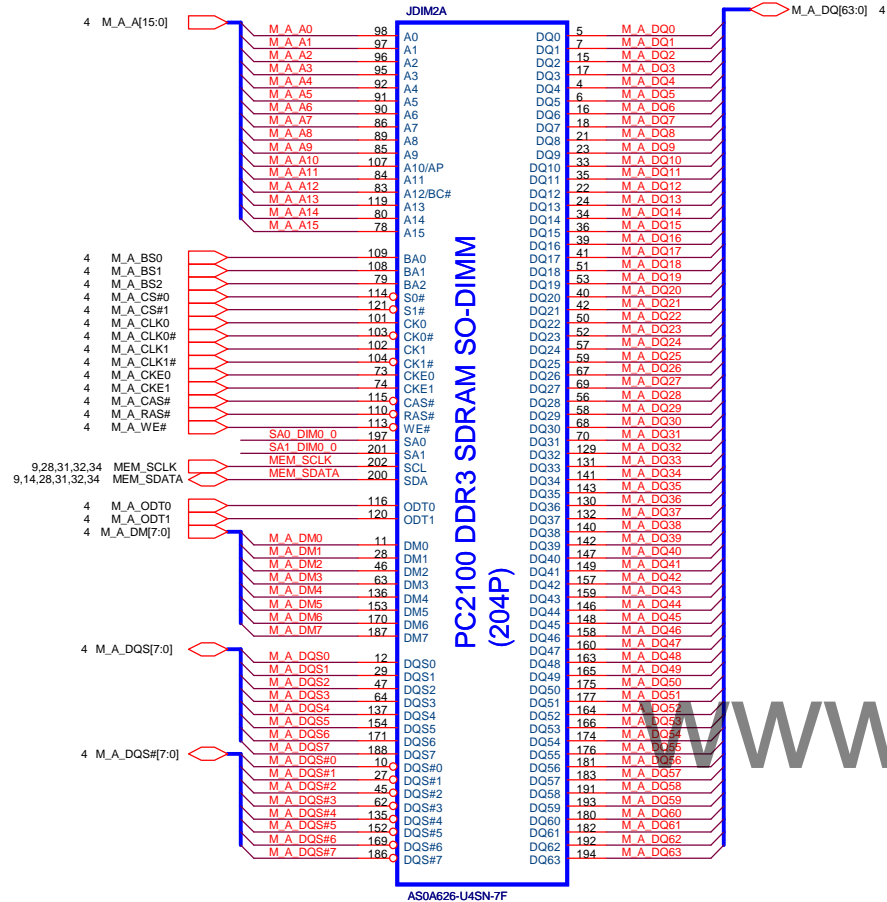
IBEX PEAK-M (GND)



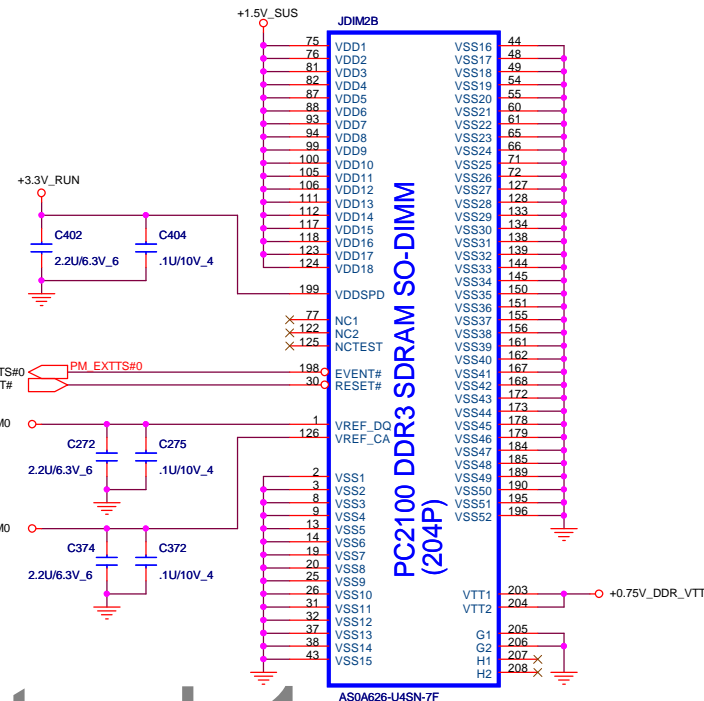
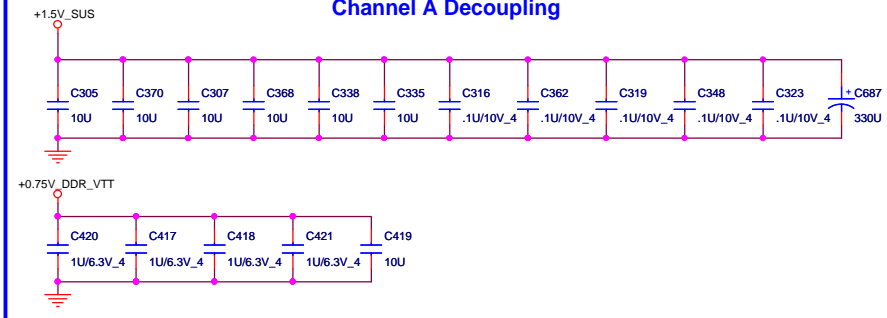
Title			
PCH 6/6(GND)			
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5/13: Change connector from Tyco to Foxconn to avoid shortage

Channel A



Channel A Decoupling



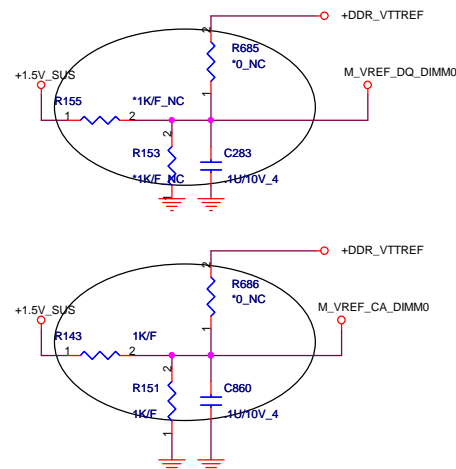
For CH A SO-DIMM VREF_DQ for M2

Delete according to Intel Design Change

M1 VREF

5/18: Separate voltage divider for M_VREF_DQ_DIMM0 and M_VREF_CA_DIMM0 to follow Intel CRB design

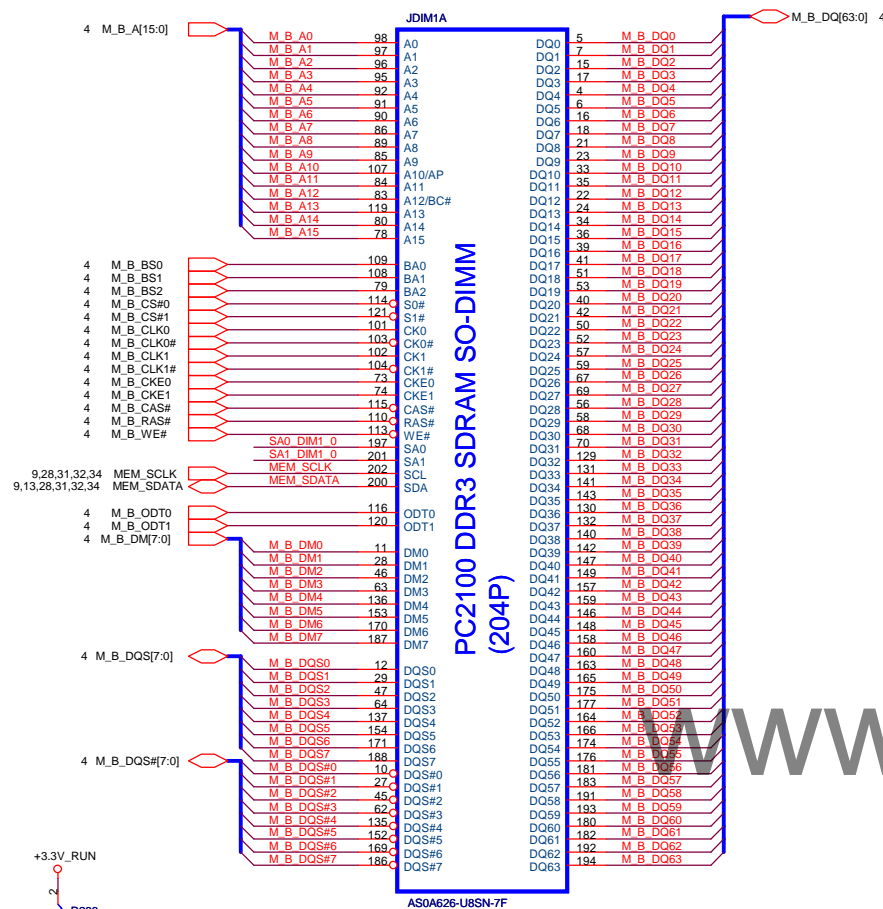
6/02: Change M1 from voltage regulator to voltage divider



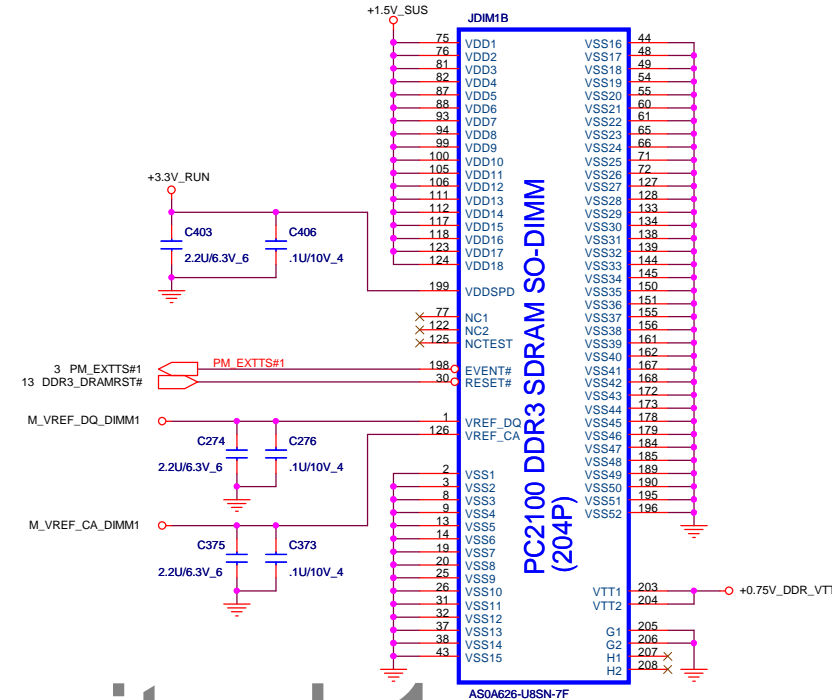
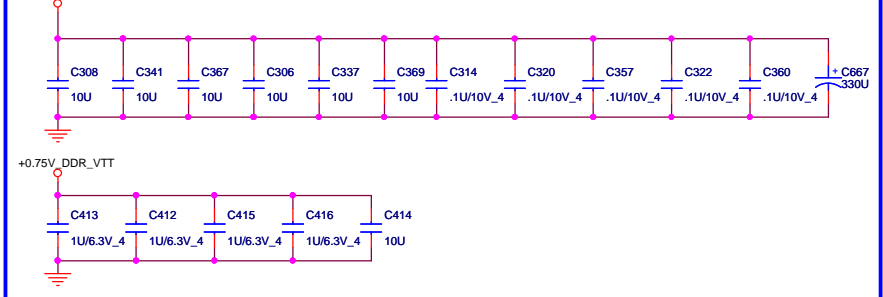
Title			DDR3 DIMM-A
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5/13: Change connector from Tyco to Foxconn to avoid shortage

Channel B



Channel B Decoupling



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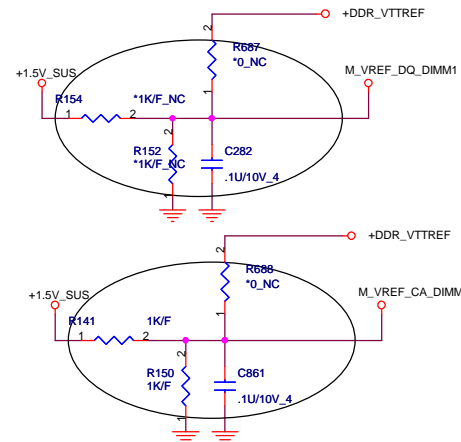
For CH B SO-DIMM VREF_DQ for M2

Delete according to Intel Design Change

M1 VREF

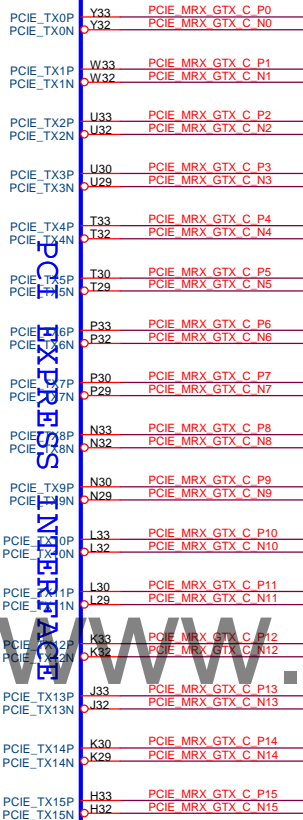
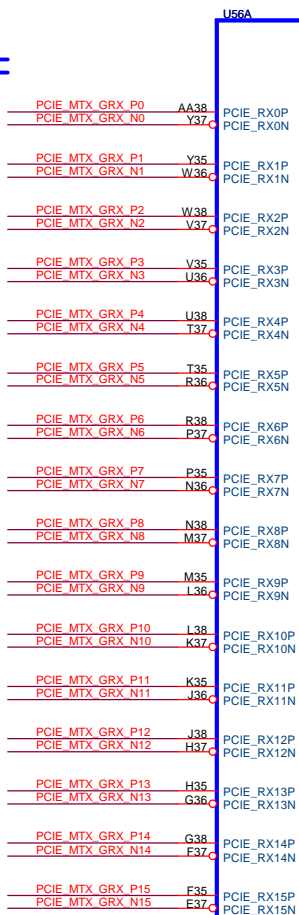
5/18: Separate voltage divider for M_VREF_DQ_DIMM1 and M_VREF_CA_DIMM1 to follow Intel CRB design

6/02: Change M1 from voltage regulator to voltage divider

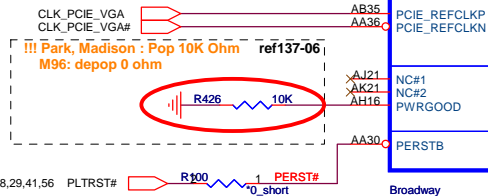


Title			DDR3 DIMM-B
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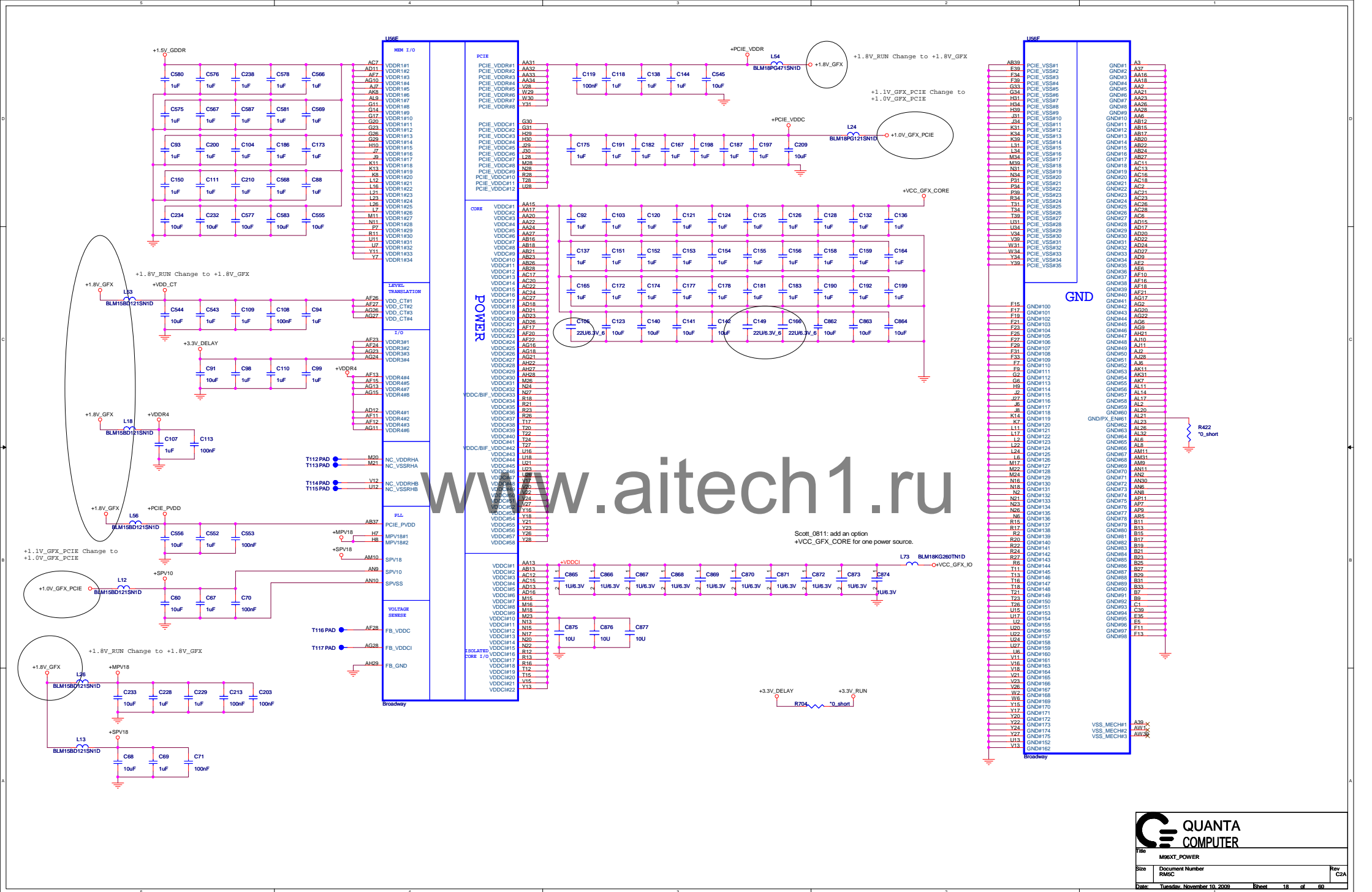
PCIE_MTX_GRX_P[0..15]
PCIE_MTX_GRX_N[0..15]



PCIE_MRX_GTX_P[0..15] 3
PCIE_MRX_GTX_N[0..15] 3



PWRGOOD should be accessible for test purposes and must be connected to ground for normal operation.



!!!
For M96/92, DPx_VDD10 = 1.1V
For M97 DPx_VDD10 = 1.0V

ref137-06

1007 for change list

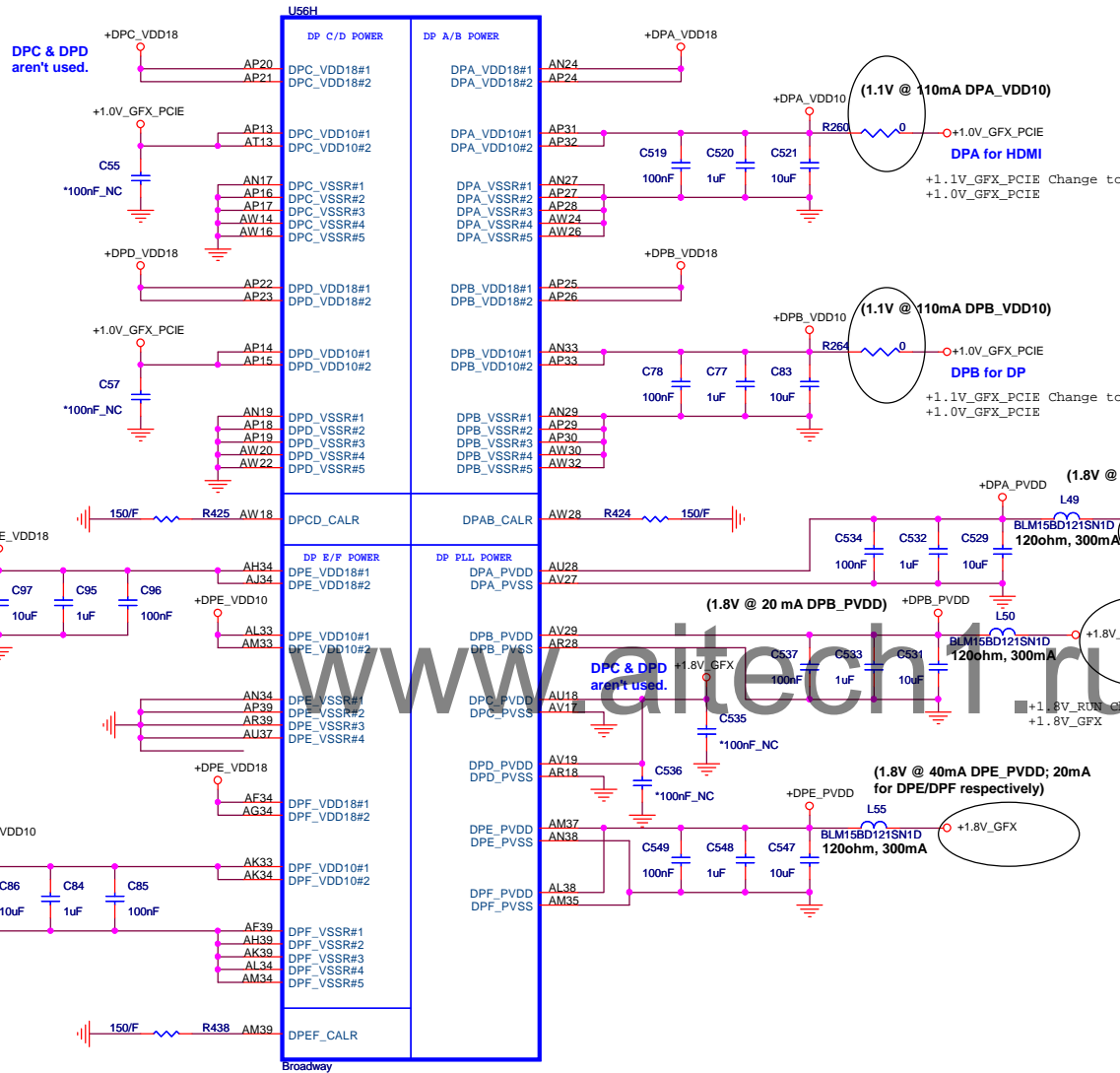
(1.8V @ 400mA DPE_VDD18;
200mA for DPE/DPF respectively)

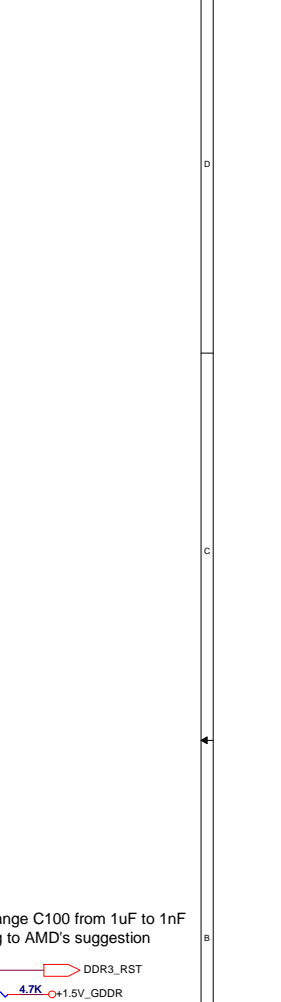
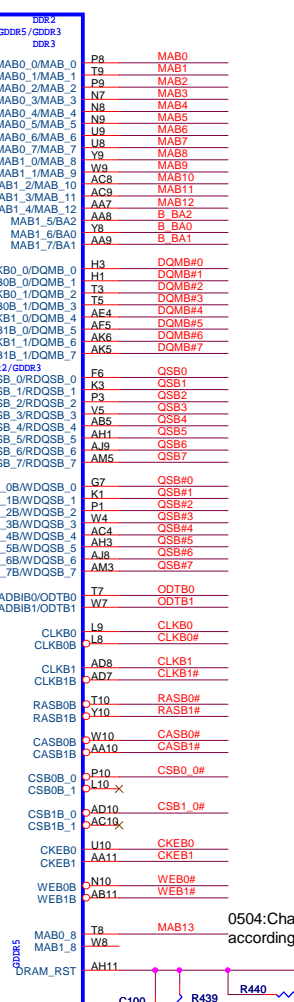
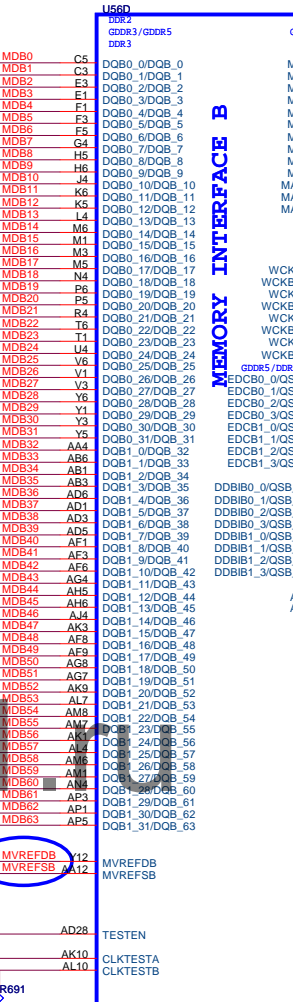
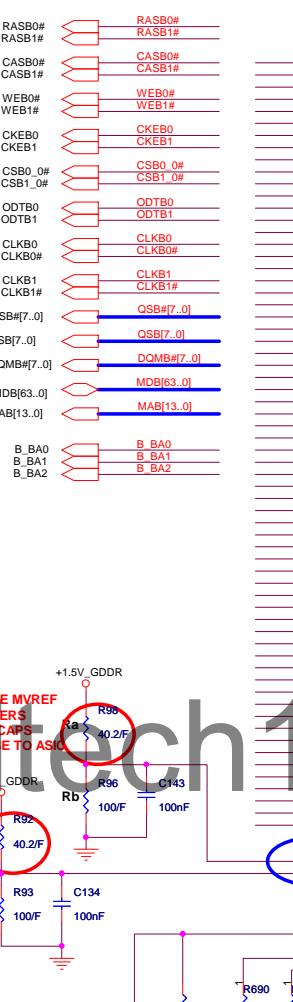
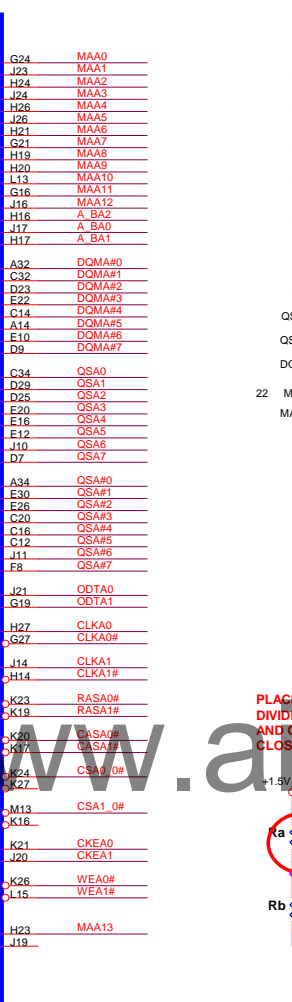
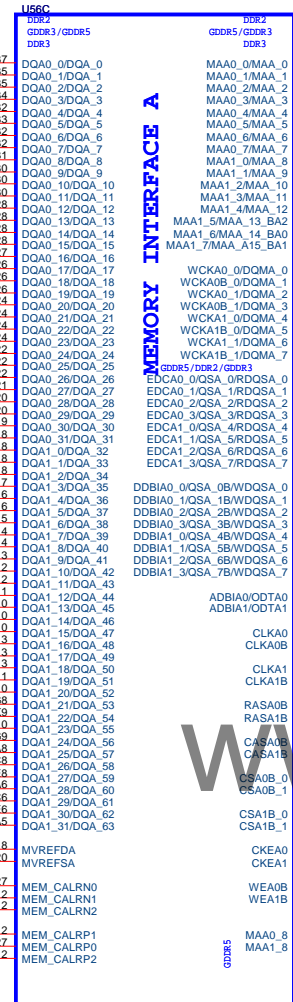
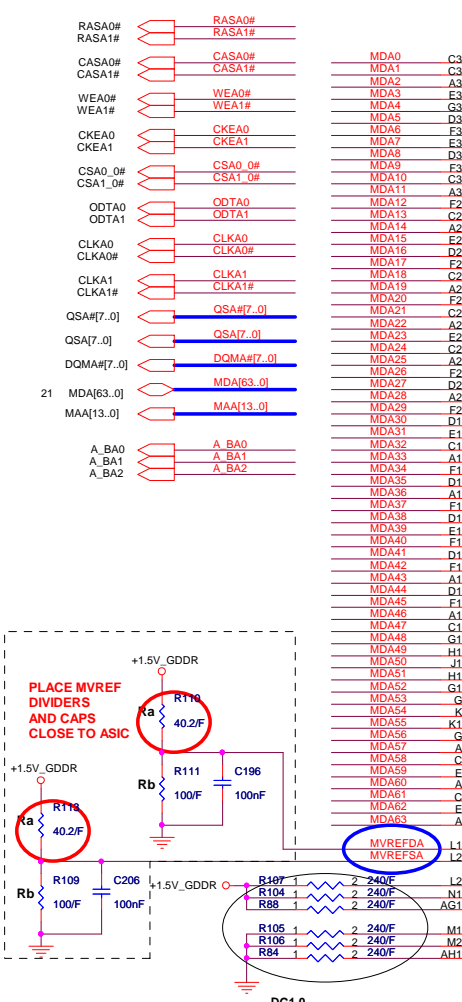
0504: Change L19 for low DCR
0.1ohm as AMD suggest.

DPE & DPF for LVDS

(1.1V @ 200mA DPE_VDD10;
100mA for DPE/DPF respectively)

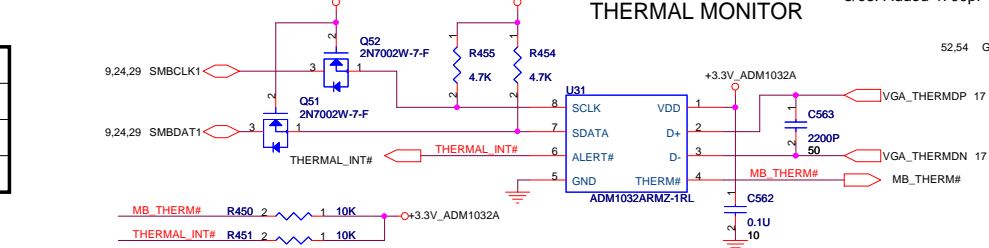
+1.1V_GFX_PCIE Change to
+1.0V_GFX_PCIE





DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



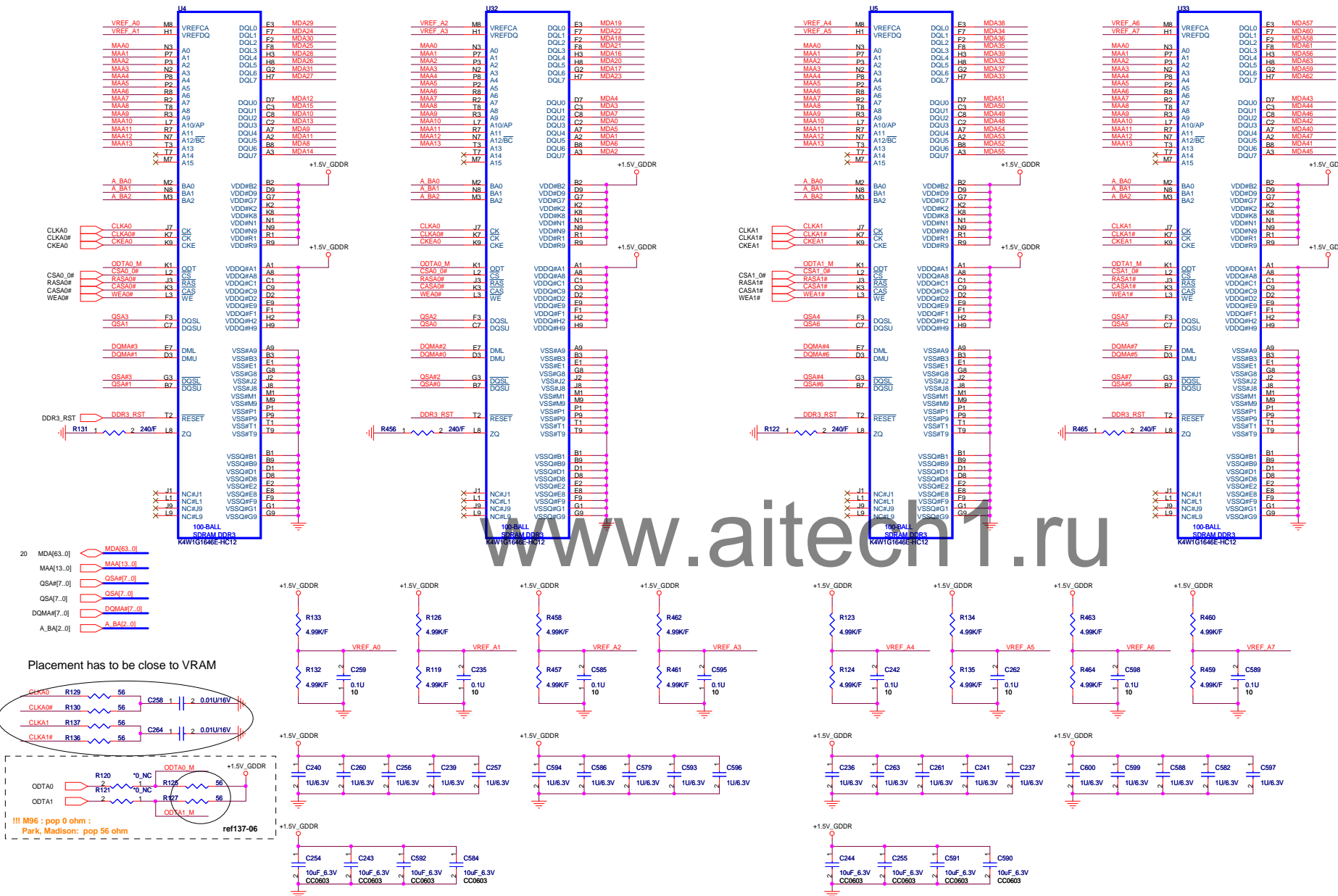
QUANTA COMPUTER

M96XT_MEMORYTHERM

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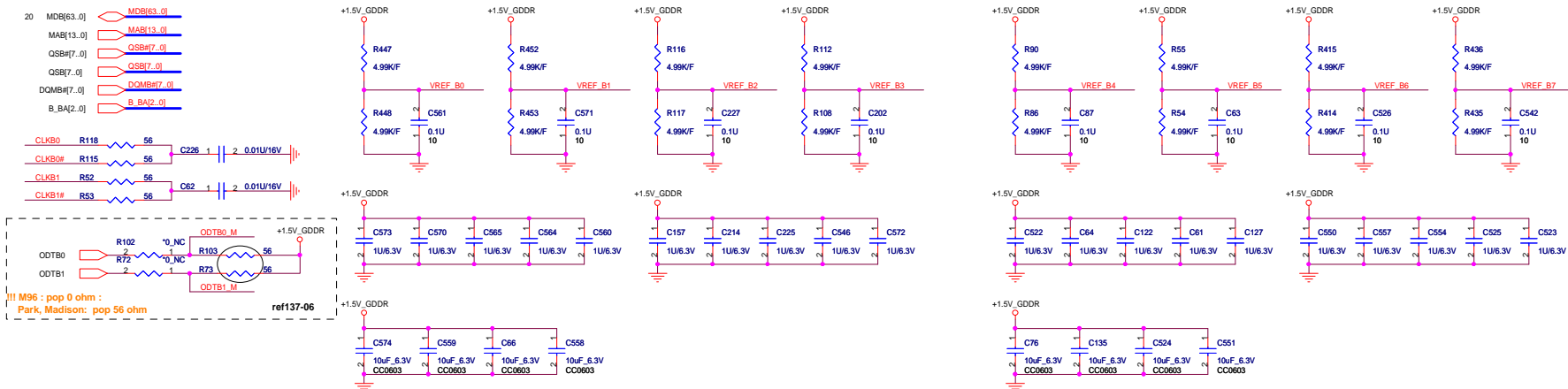
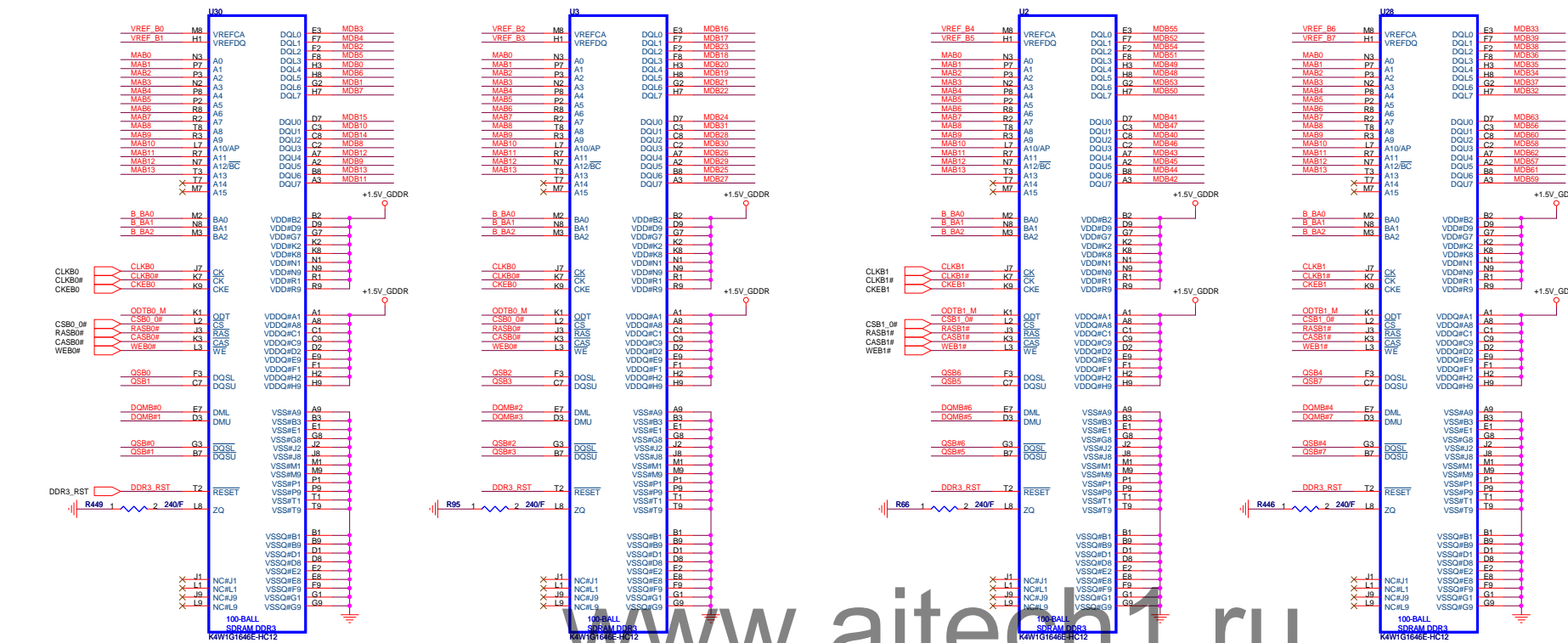
DDR3 64MX16, CH A : 512MB



File: M96XT_DDR3_A_512M

Size: Document Number
RMSD
Date: Monday, November 09, 2009 Sheet: 21 of 60

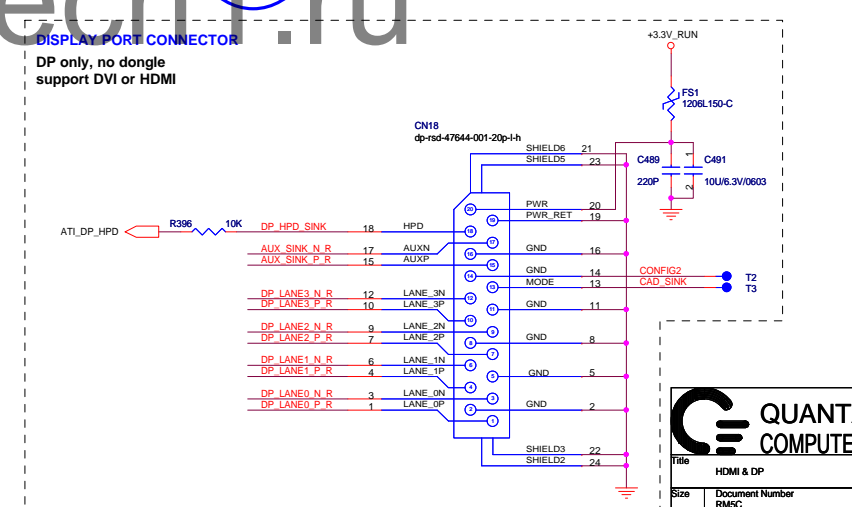
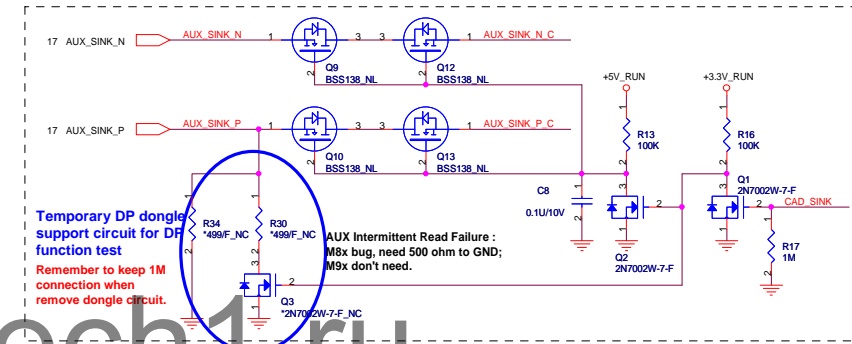
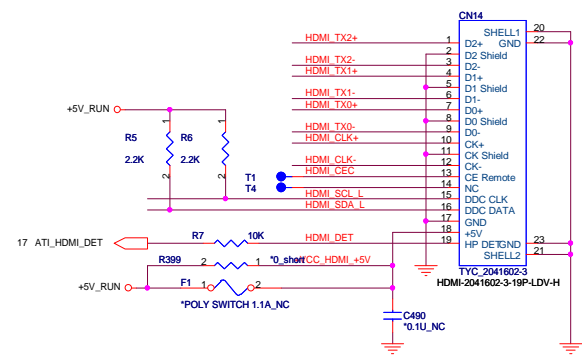
DDR3 64MX16, CH B : 512MB



File: M96XT_DDR3_B_512M

Size	Document Number	Rev
	RMC	C2A

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Delete EMI ESD IC for EMI asked HDMI signals link to CONN directly.

Temporary DP dongle support circuit for DP function test

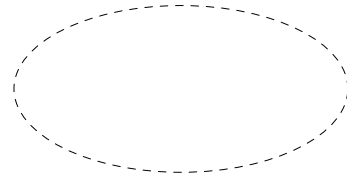
Remember to keep 1M connection when remove dongle circuit.

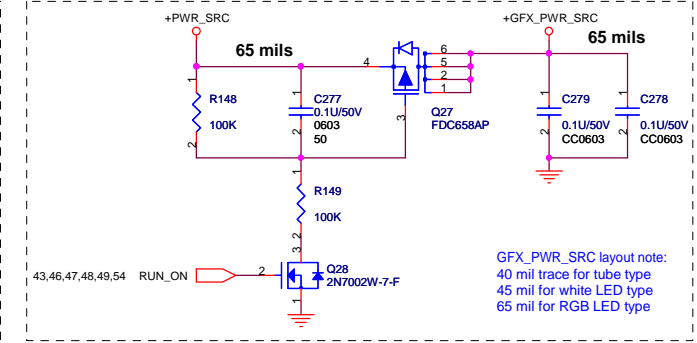
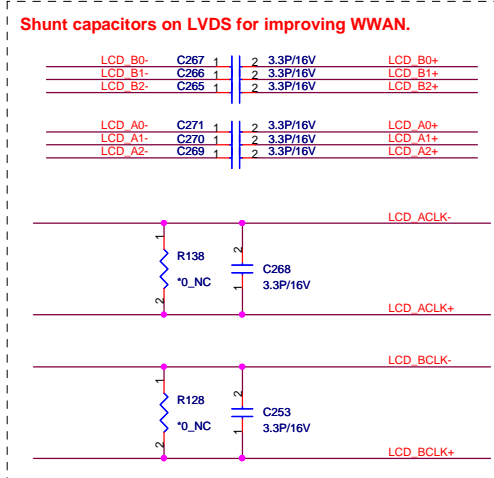
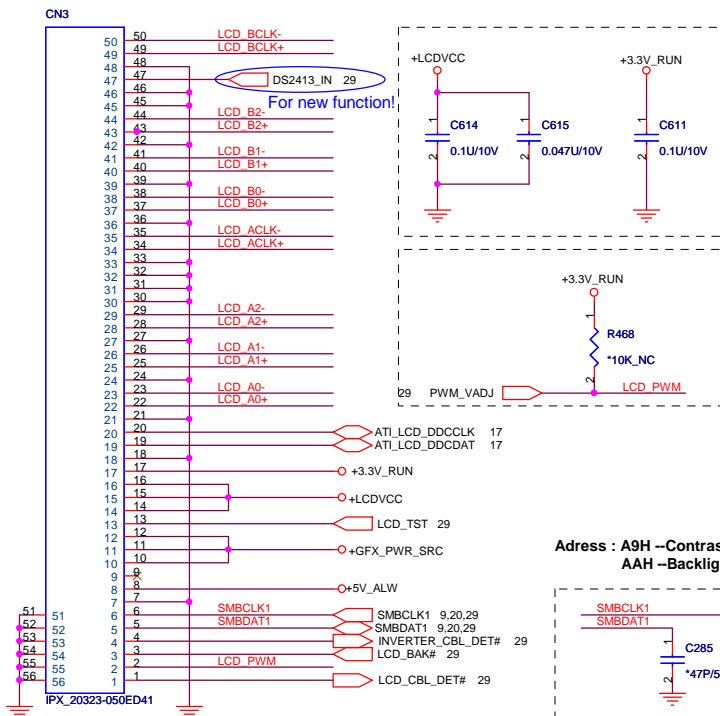
AUX Intermittent Read Failure :
M8x bug, need 500 ohm to GND;
M9x don't need.

DISPLAY PORT CONNECTOR

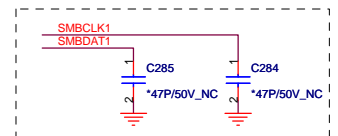
DP only, no dongle
support DVI or HDMI

Scott_0703:Delete ESD Clamp U23,U24,U25 as EMI suggestion.

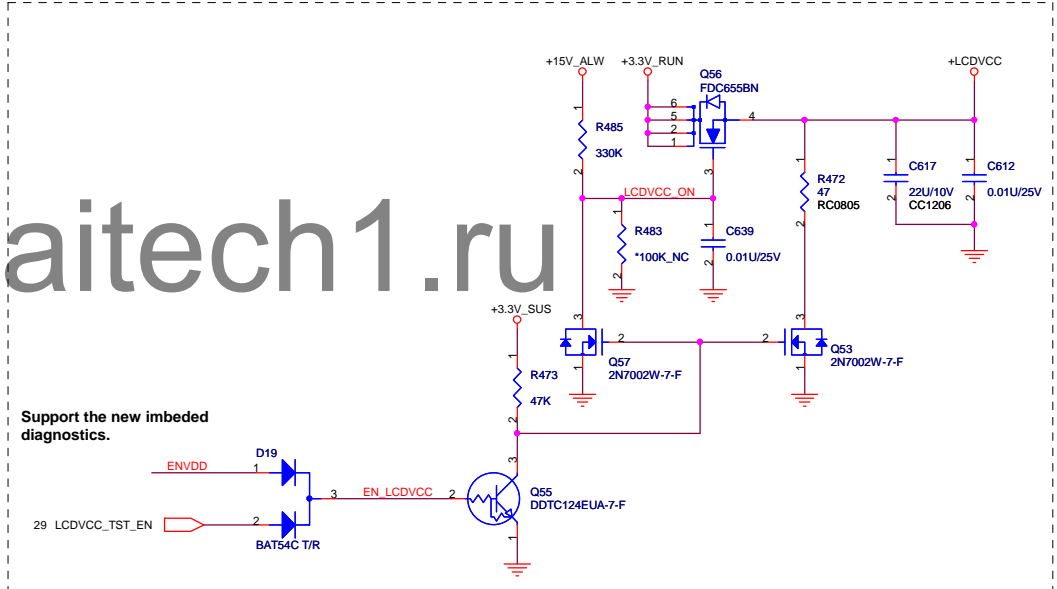
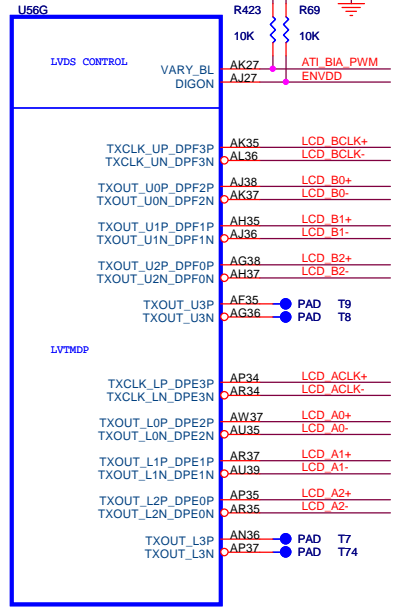


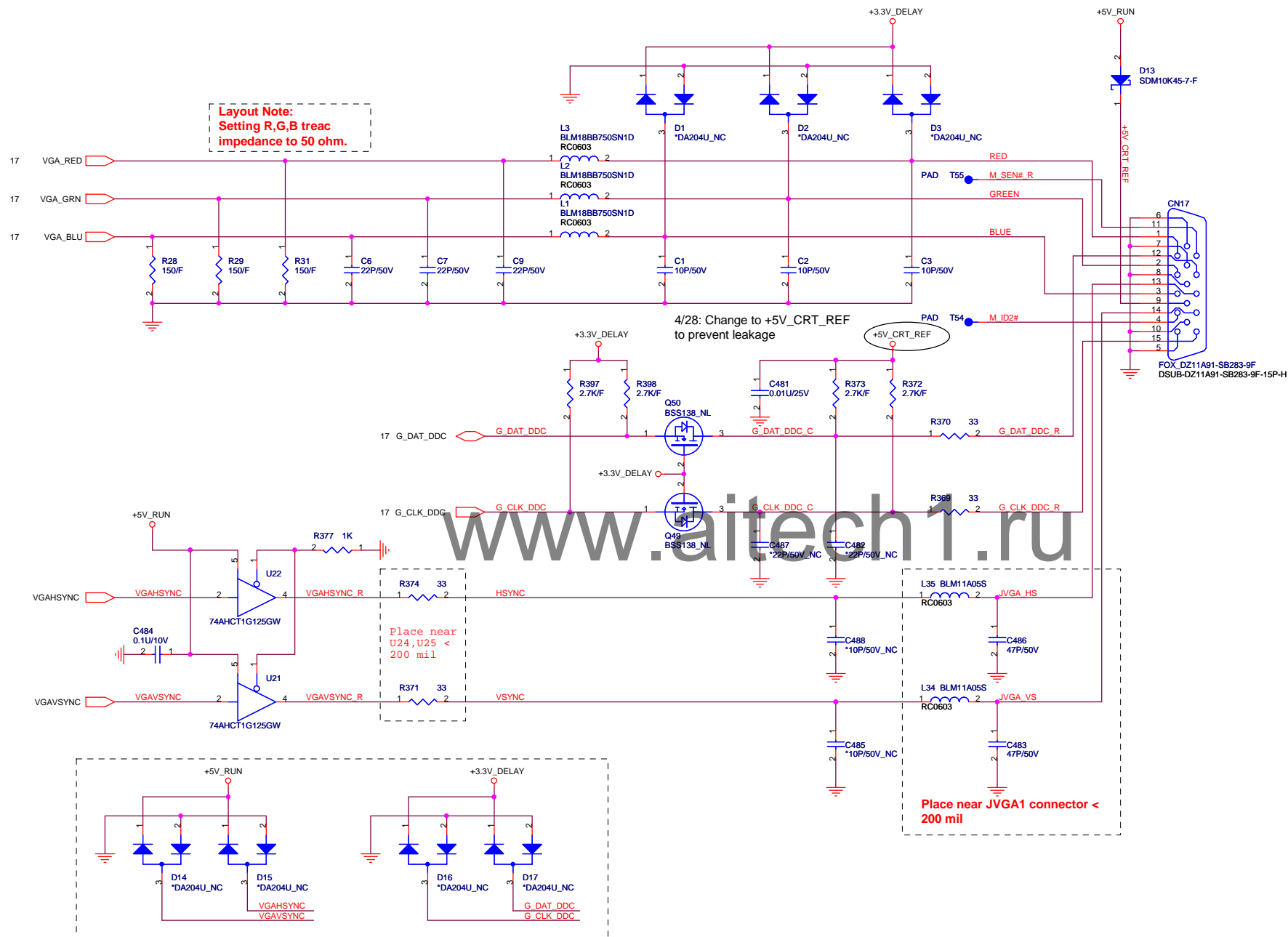


Address : A9H --Contrast
AAH --Backlight

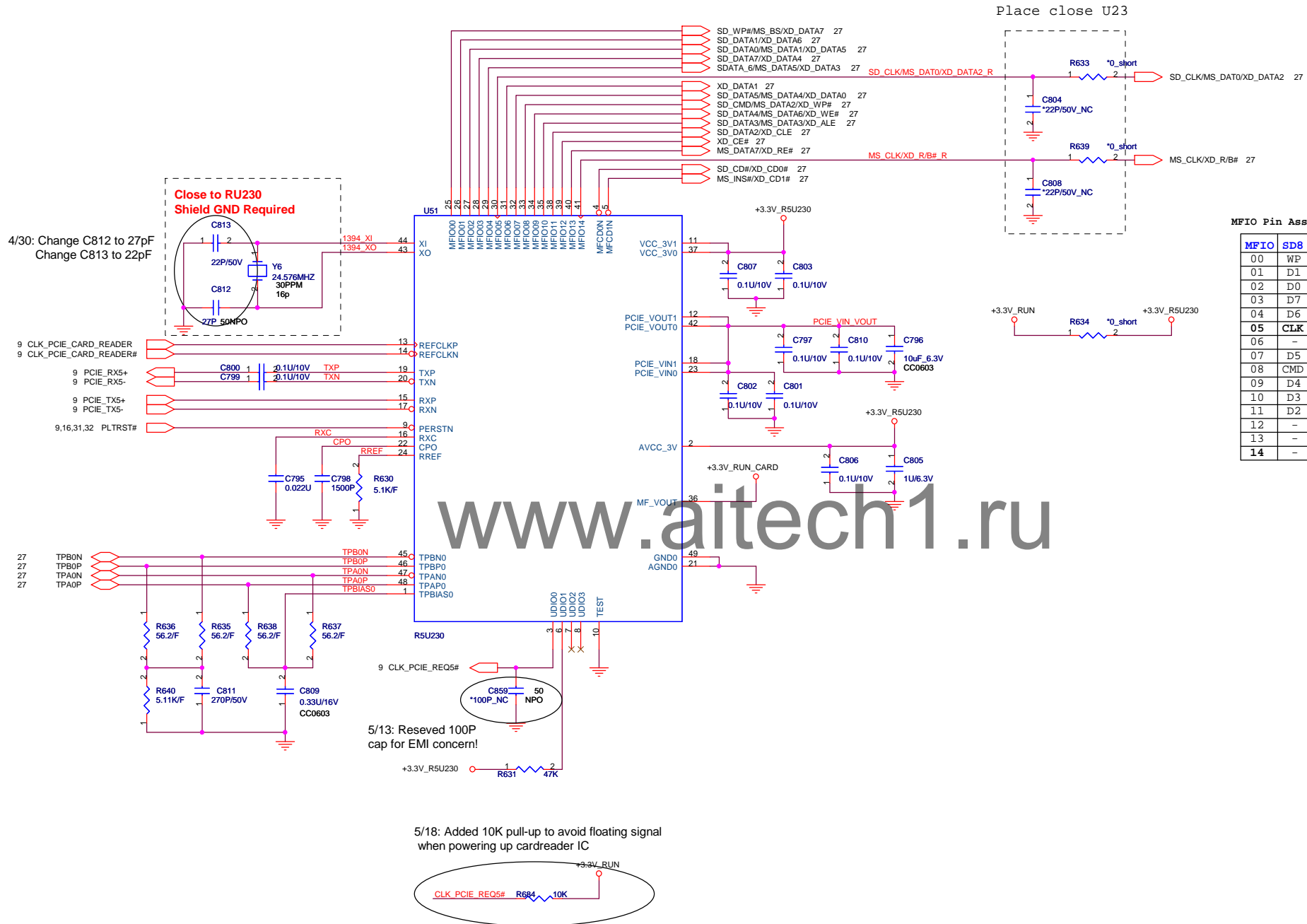


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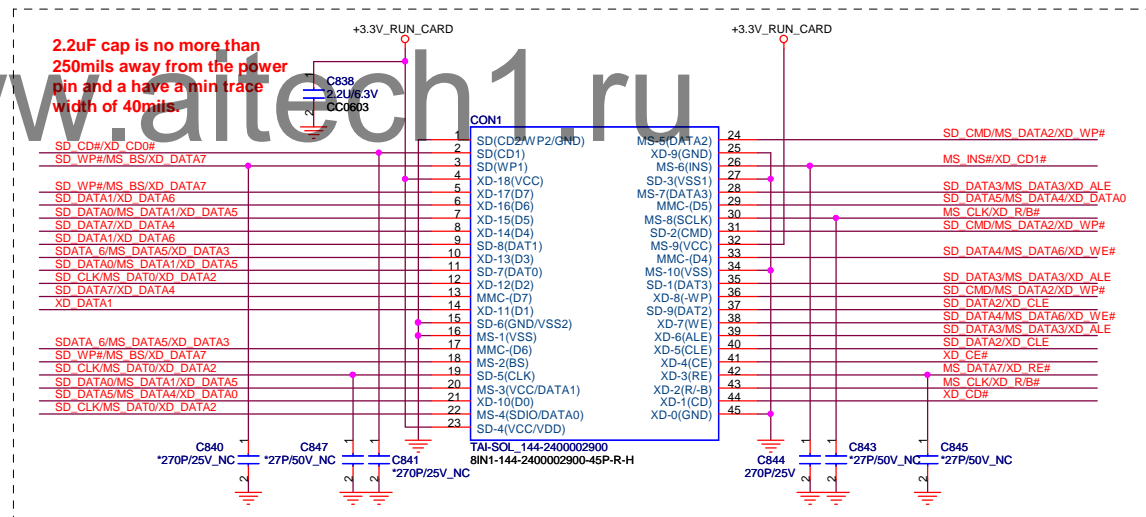
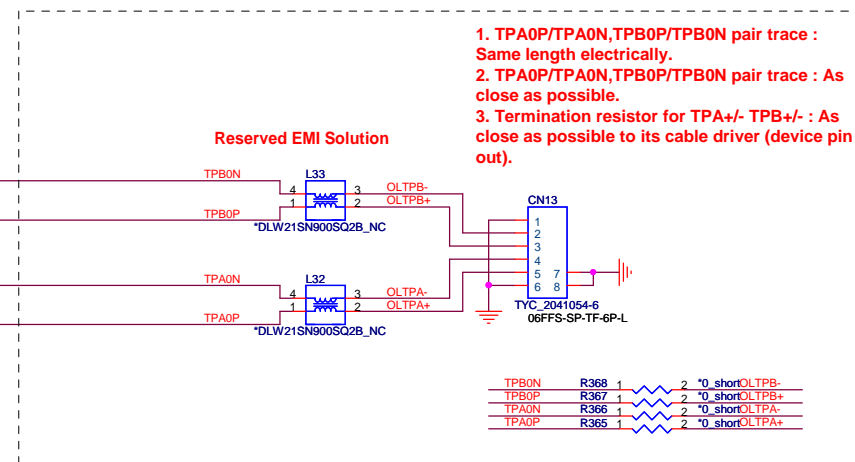
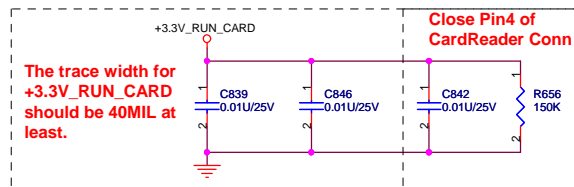
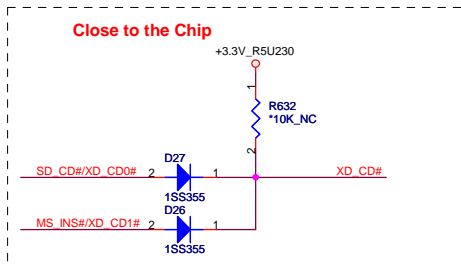
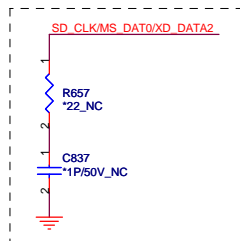
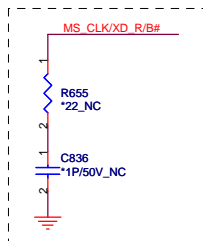


Title CRT CONN		
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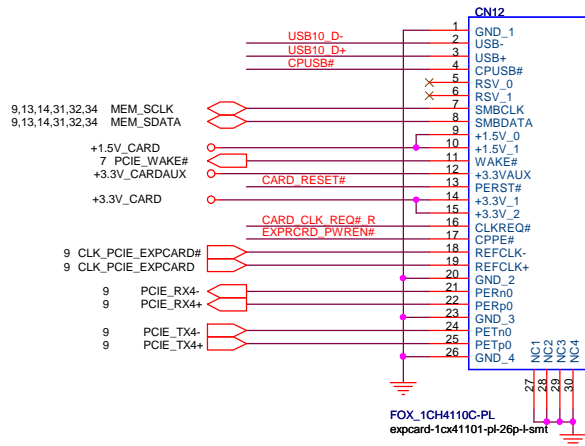


26 SD_WP#/MS_BS/XD_DATA7
 26 SD_DATA1/XD_DATA6
 26 SD_DATA0/MS_DATA1/XD_DATA5
 26 SD_DATA7/XD_DATA4
 26 SDATA_6/MS_DATA5/XD_DATA3
 26 SD_CLK/MS_DATA0/XD_DATA2
 26 XD_DATA1
 26 SD_DATA5/MS_DATA4/XD_DATA0
 26 SD_CMD/MS_DATA2/XD_WP#
 26 SD_DATA4/MS_DATA6/XD_WE#
 26 SD_DATA3/MS_DATA3/XD_ALE
 26 SD_DATA2/XD_CLE
 26 XD_CE#
 26 MS_DATA7/XD_RE#
 26 MS_CLK/XD_R/B#
 26 SD_CD#/XD_CD0#
 26 MS_INS#/XD_CD1#

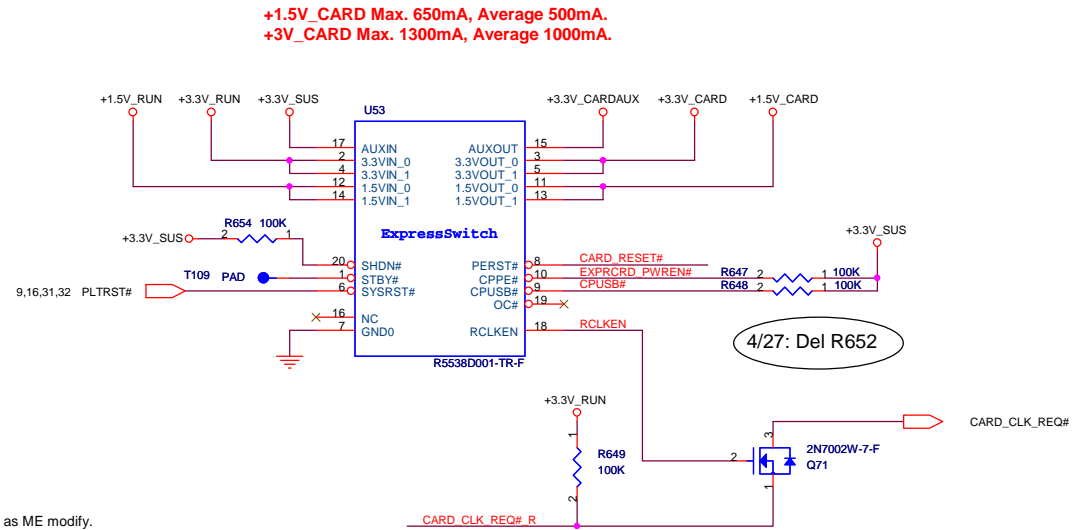
SD_WP#/MS_BS/XD_DATA7
 SD_DATA1/XD_DATA6
 SD_DATA0/MS_DATA1/XD_DATA5
 SD_DATA7/XD_DATA4
 SDATA_6/MS_DATA5/XD_DATA3
 SD_CLK/MS_DATA0/XD_DATA2
 XD_DATA1
 SD_DATA5/MS_DATA4/XD_DATA0
 SD_CMD/MS_DATA2/XD_WP#
 SD_DATA4/MS_DATA6/XD_WE#
 SD_DATA3/MS_DATA3/XD_ALE
 SD_DATA2/XD_CLE
 XD_CE#
 MS_DATA7/XD_RE#
 MS_CLK/XD_R/B#
 SD_CD#/XD_CD0#
 MS_INS#/XD_CD1#



Express Card



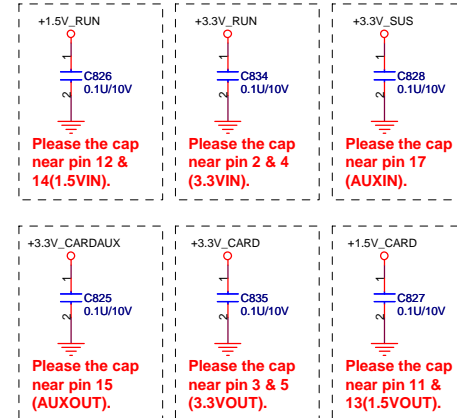
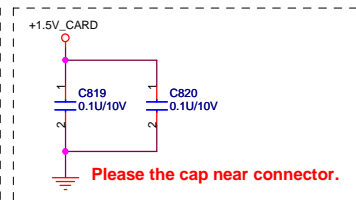
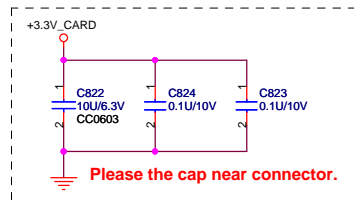
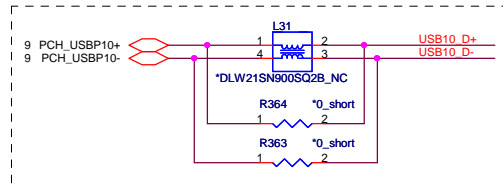
Scott_0813: Change CN12 F/P to expcard-1cx41101-pl-26p-l-smt.



4/27: Del R652

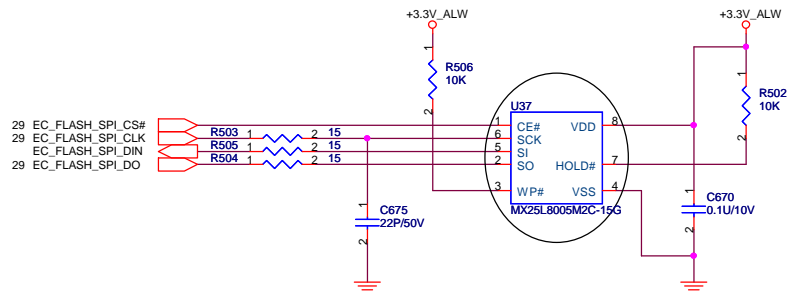
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PCI-Express TX and RX direct to connector.

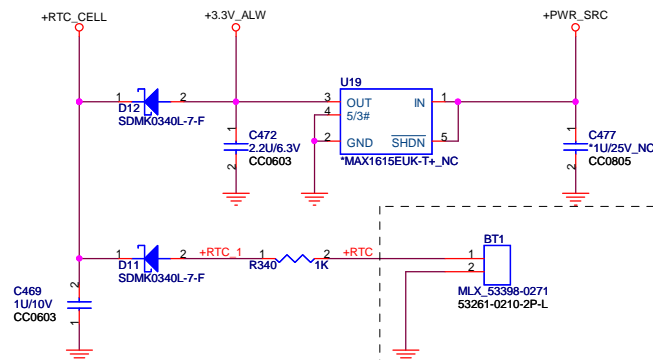


EC SPI ROM, 8Mbit (1M Byte)

5/12: Change U37 from 2MB to 1MB according to BIOS request!

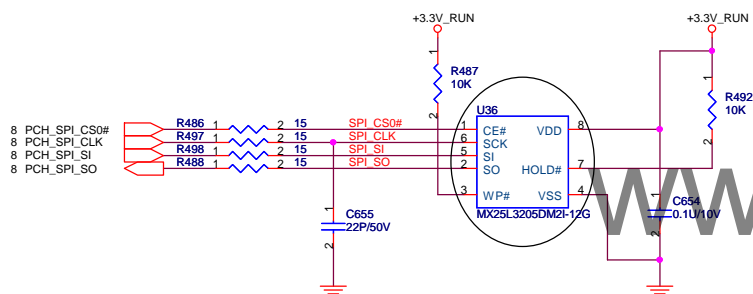


RTC BATTERY

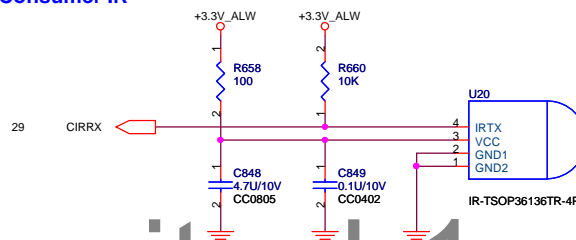


PCH SPI ROM, (4M Byte)

5/12: Change U36 from 2MB to 4MB according to BIOS request!



Consumer IR



Title			FLASH/ RTC/ CIR
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Mini Card Nut

H21
Mini Card Align (H6.6)



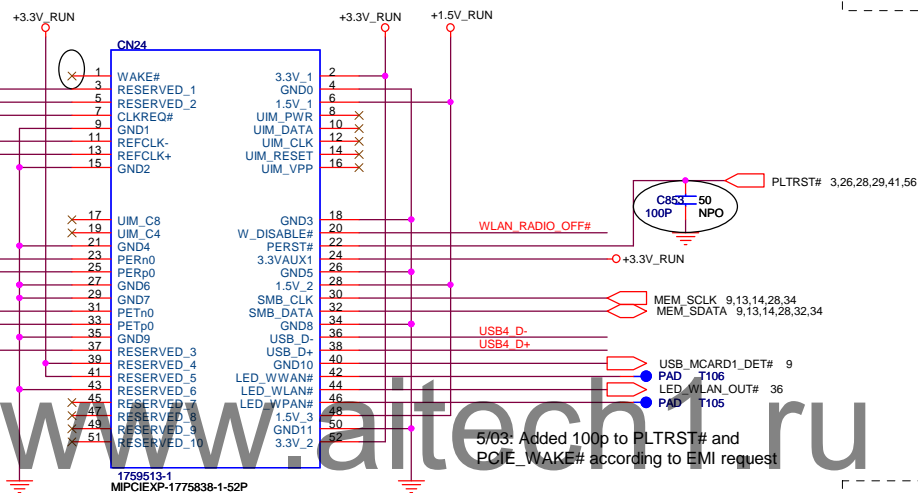
MiniCard WLAN Connector

5/15: Change WAKE# to NC as it is not required

COEX2_WLAN_ACTIVE
COEX1_BT_ACTIVE_MINI
MINI1CLK_REQ#

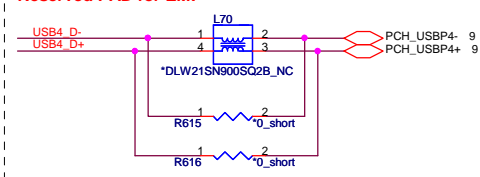
PCI-Express TX and RX
direct to connector

9 PCIE_RX2-
9 PCIE_RX2+
9 PCIE_TX2-
9 PCIE_TX2+
10 PCIE_MCARD1_DET#

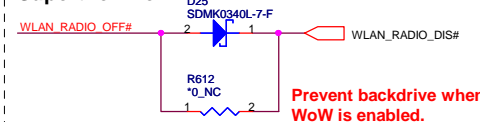


5/03: Added 100p to PLTRST# and PCIE_WAKE# according to EMI request

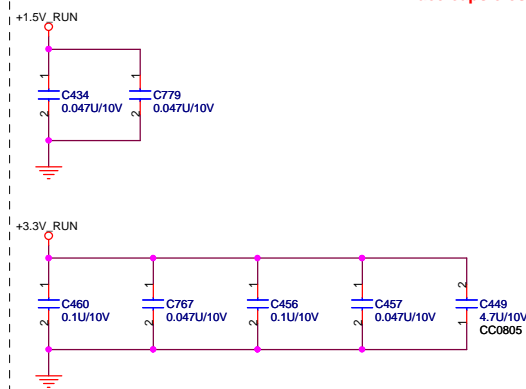
Reserved PAD for EMI



Support for WoW



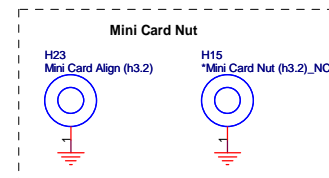
Place caps close to connector.



Title MINI-CARD (WLAN)		
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5/15: Change WAKE# to NC as it is not required

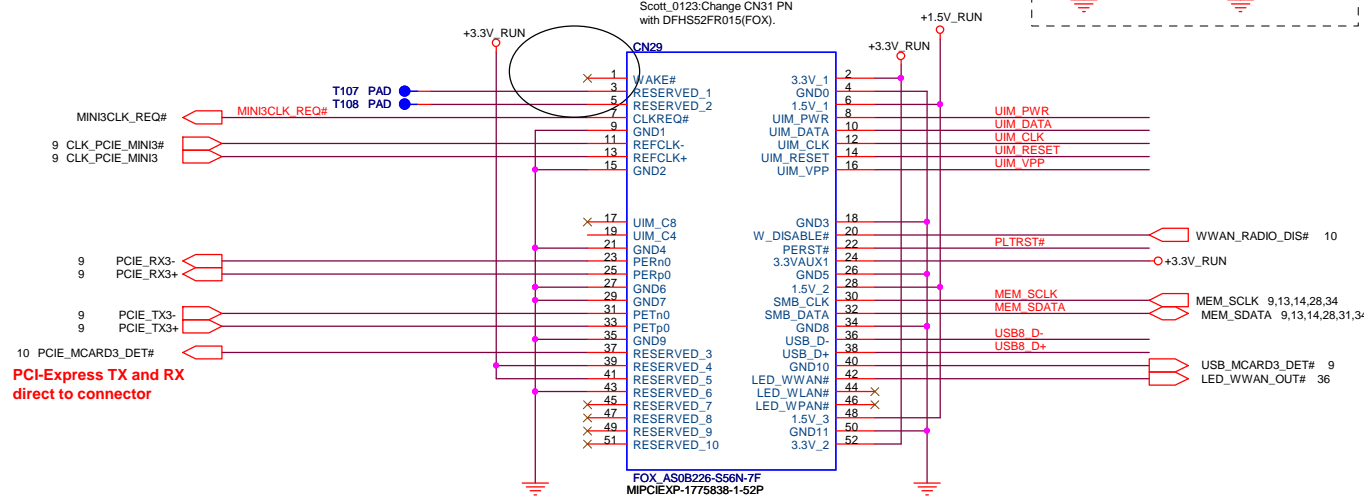
MiniCard WWAN Connector



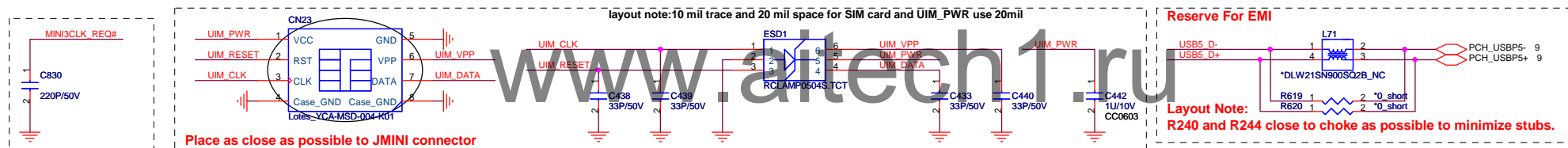
Layout Note:

Place caps close to connector.

The diagram illustrates the placement of decoupling capacitors for two power rails: +1.5V_RUN and +3.3V_RUN. The +1.5V_RUN rail is connected to a connector and has two capacitors, C816 and C817, placed close to the connector. The +3.3V_RUN rail is also connected to a connector and has five capacitors, C817, C833, C818, C829, and C832, placed close to the connector. The capacitors are labeled with their values and ratings: C816 (0.047U/10V), C817 (33P/50V), C833 (0.047U/10V), C818 (33P/50V), C829 (0.047U/10V), and C832 (330U/6.3V CC7343).



5/13: Change SIM card connector to Lotes

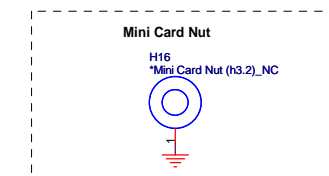


Layout Note:
R240 and R244 close to choke as possible to minimize stubs

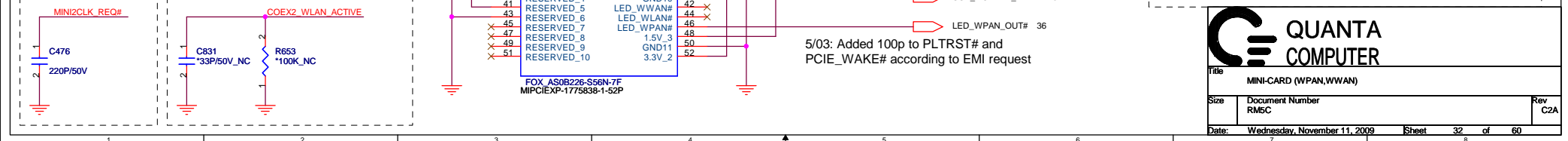
Layout Note: R240 and R244 close to choke as possible to minimize stubs.

MiniCard Robson, BT. UWB Connector

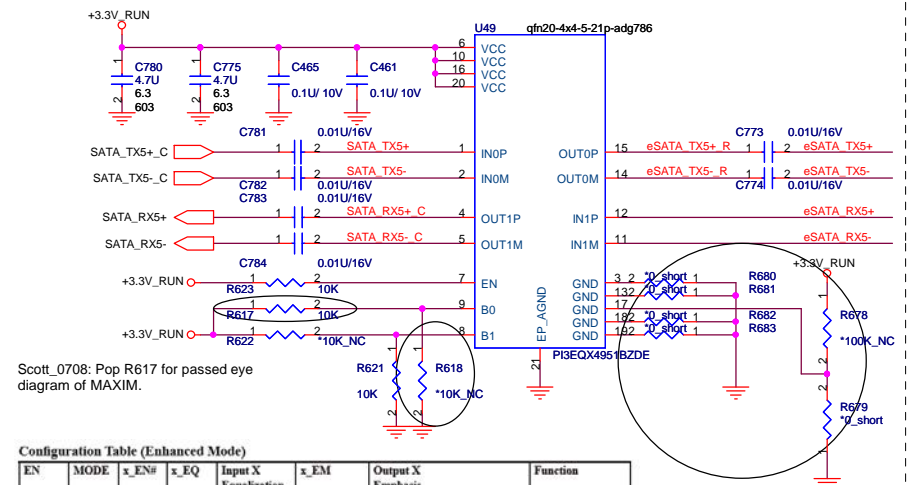
Scott_0123:Change CN2
PN with DFHS52FR015.



5/03: Added 100p to PLTRST# and
PCIE_WAKE# according to EMI request



eSATA Re-driver IC

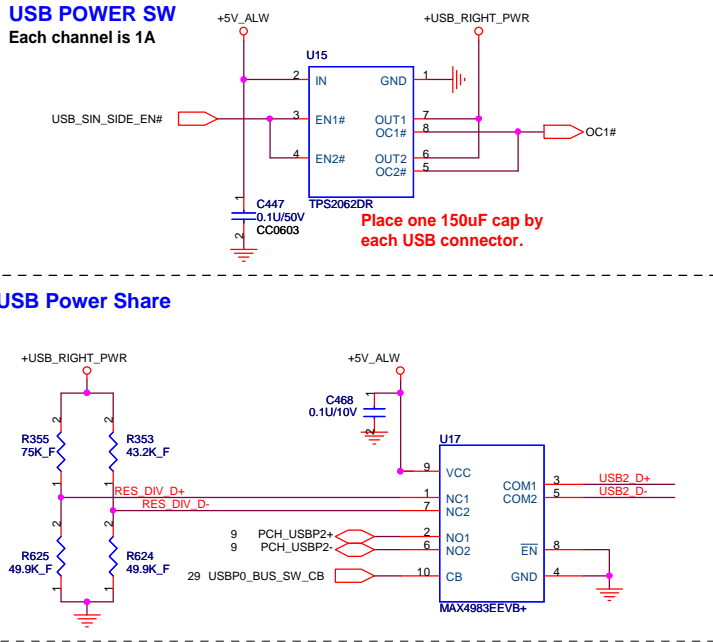


Configuration Table (Enhanced Mode)

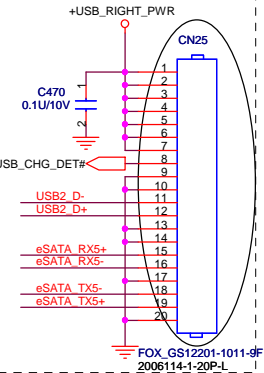
EN	MODE	x_EN#	x_EQ	Input X Equalization	x_EM	Output X Emphasis	Function
0	X	X	X	n/a	X	n/a	Chip Power Down
1	1	1	X	n/a	X	n/a	Chip enabled, Channel x disabled
1	1	0	0	2.5dB	1.1K to 15K resistor	Resistor Controlled, 6dB to 0dB (0)	Chip and channel enabled, low input equalization
1	1	0	1	6.5dB	1.1K to 15K resistor	Resistor Controlled, 6dB to 0dB (0)	Chip and channel enabled, high input equalization

5/11: Reserved 0 ohms for Pericom enhanced mode select,
5/12: Change IC to Pericom as Maxim failed EA test
6/23: NC according to Pericom recommendation!

USB POWER SW
Each channel is 1A

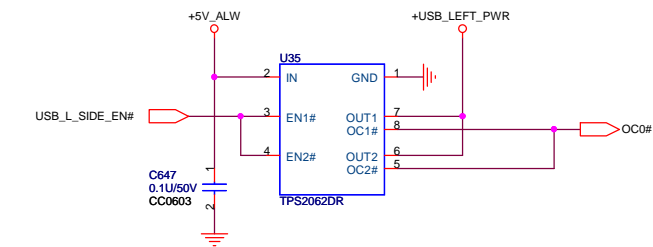


eSATA CONN



5/13: Change Connector to Foxconn to avoid material shortage for Tyco

USB POWER SW
Each channel is 1A



TV module

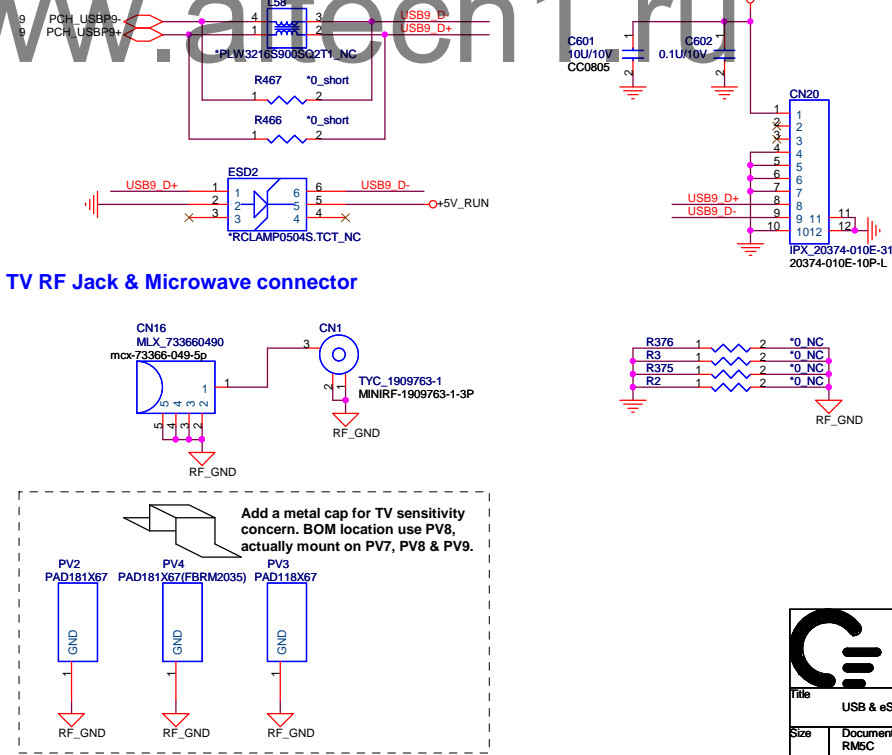


Diagram illustrating the SATA interface connection for the FOX GS12201-1011-9F board (2006114-1-20P-L).

The diagram shows the connection of the CN21 connector to the SATA controller and power pins.

Pin Connections:

- Pin 1:** GND1
- Pin 2:** RXP
- Pin 3:** RXN
- Pin 4:** GND2
- Pin 5:** TXN
- Pin 6:** TXP
- Pin 7:** GND3
- Pin 8:** 3.3V_0
- Pin 9:** 3.3V_1
- Pin 10:** 3.3V_2
- Pin 11:** GND4
- Pin 12:** GND5
- Pin 13:** GND6
- Pin 14:** 5V_0
- Pin 15:** 5V_1
- Pin 16:** 5V_2
- Pin 17:** GND7
- Pin 18:** GND8
- Pin 19:** 12V_0
- Pin 20:** 12V_1
- Pin 21:** GND9
- Pin 22:** GND10
- Pin 23:** GND11
- Pin 24:** GND12

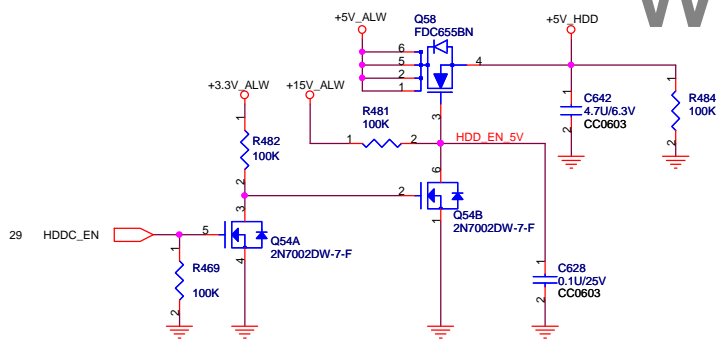
SATA Signal Connections:

- SATA TX0+:** Connected to C292 (Pin 2) and C293 (Pin 3).
- SATA TX0-:** Connected to C292 (Pin 2) and C293 (Pin 3).
- SATA RXN0 C:** Connected to C291 (Pin 5) and C290 (Pin 6).
- SATA RXN0:** Connected to C291 (Pin 5) and C290 (Pin 6).
- SATA TXP:** Connected to C291 (Pin 5) and C290 (Pin 6).
- SATA RX0+:** Connected to C291 (Pin 5) and C290 (Pin 6).
- SATA RX0-:** Connected to C291 (Pin 5) and C290 (Pin 6).

Power Connections:

- 3.3V_RUN:** Connected to Pin 8.
- 5V_HDD:** Connected to Pin 14.

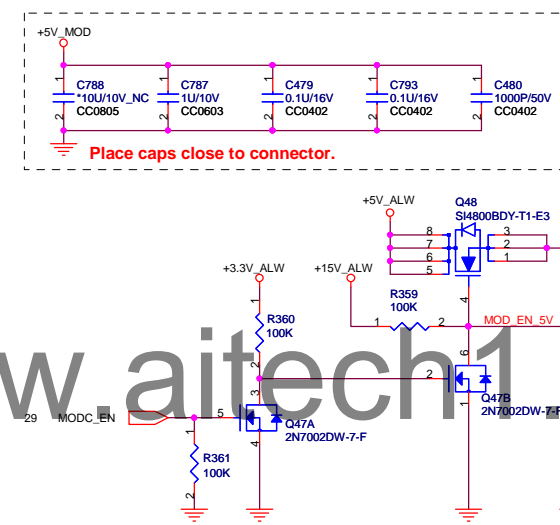
Board Identification: FOX GS12201-1011-9F, 2006114-1-20P-L.

[illegible]

CN28

Pin	Signal	Connector	Signal	Connector	Signal	Connector
1	GND1	1	SATA TX1+	C792	2	1 0.01U/16V
2	RXP	2	SATA TX1-	C791	2	1 0.01U/16V
3	RXN	3				
4	GND2	4	SATA RX1N C	C790	1	2 0.01U/25V
5	TXN	5	SATA RX1P C	C789	1	2 0.01U/25V
6	TXP	6				
7	GND3	7				
8	DP	8				
9	5V_0	9				
10	5V_1	10				
11	MD	11				
12	GND	12				
13	GND	13				

MLX 47645-2000
SATA-47645-2000-13P-L-H



To Daughter Board connector

Solid White = System On, Normal Activity
Off= System off (system off or hibernate);
"Breathing White" = System in Standby (S3);

Power Button

Speaker

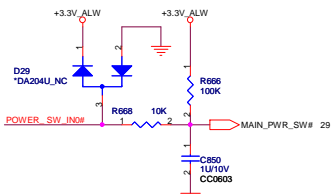
KB LED

Touch Pad

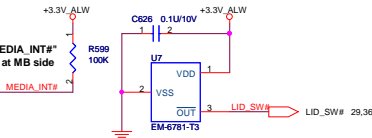
Media Button

Scott_0123: Change CN8 PN with DFHD32MR003 (With mylar)

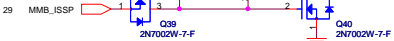
Power Button



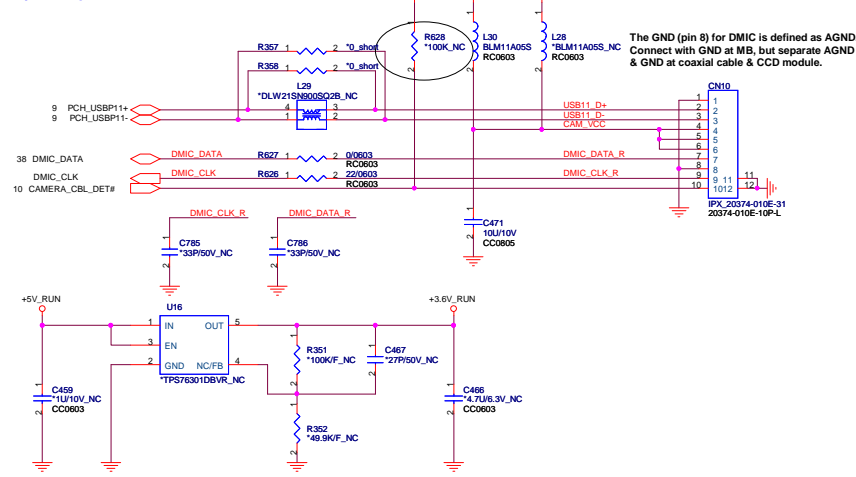
Hall Switch



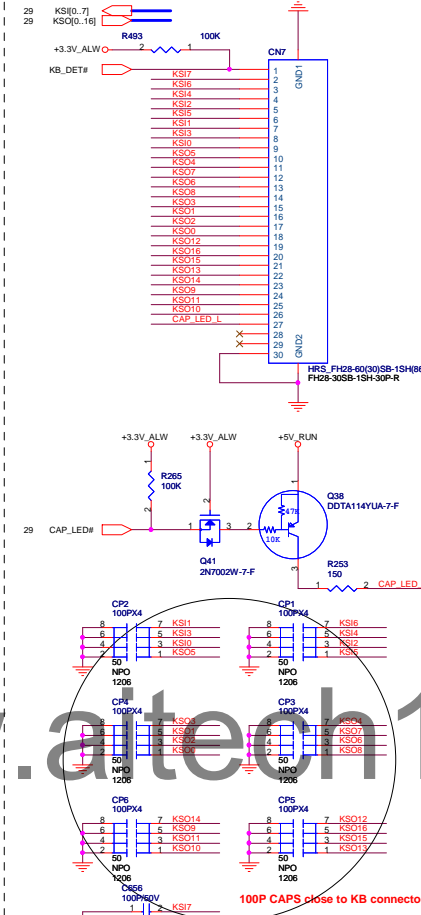
Active high for ISSP reset



Array Microphone & Camera



KEYBOARD CONNECTOR



5/03: Populate according to EMI request!
5/12: Change from CA110084N04 to CA110084N39 due to material shortage!



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Hinge & Power Button board LED (PWR/Battery indicator)

Hinge LED

Solid White= System On, Normal Activity
Solid White= Charging (system on);
Solid White= Charging (system off or hibernate and battery charge <90%);
Off= Charging (system off or hibernate and battery charge > 90%);
"Breathing White " = System in Standby (S3);
Off = System Off (or in Hibernate);

Scott_0912: Change to +5V_ALW power rail for solve LED blinking issue.

Power button board LED:

Solid White = System On, Normal Activity
Off= System off (system off or hibernate);
"Breathing White " = System in Standby (S3)

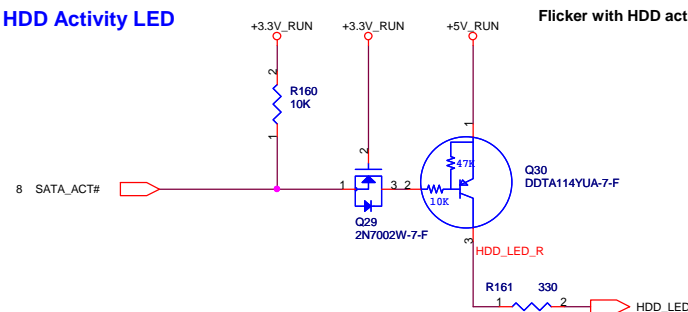
Hinge LED:

Flashing Amber = Low Battery (S0 and S3 and no AC) when battery charge <10%
Flash rate = on 1/4 sec., off 3/4 sec.

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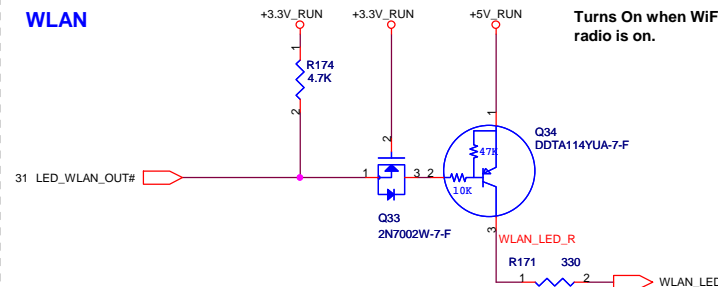
HDD Activity LED

Flicker with HDD activity.



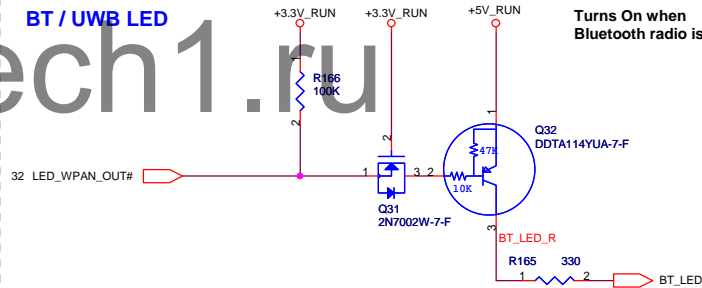
WLAN

Turns On when WiFi radio is on.



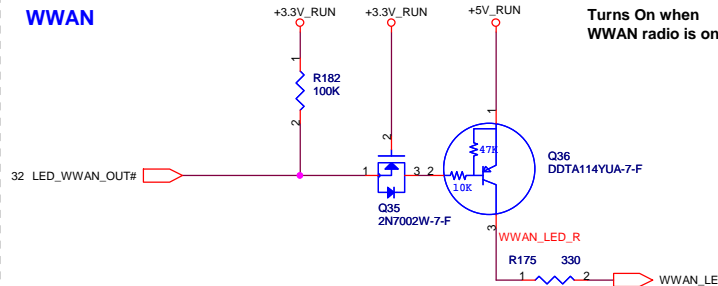
BT / UWB LED

Turns On when Bluetooth radio is on.



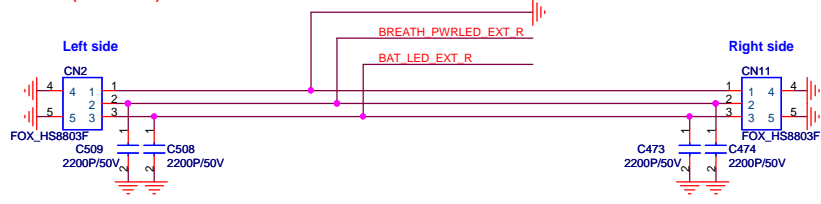
WWAN

Turns On when WWAN radio is on.



Hinge LED (PWR/Battery indicator)

L-C filter (reserve R-C) for EMI

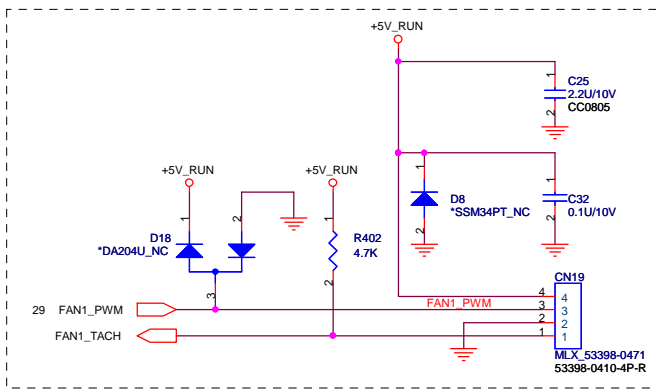


Solid White= System On, Normal Activity
Solid White= Charging (system on);
Solid White= Charging (system off or hibernate and battery charge <90%);
Off= Charging (system off or hibernate and battery charge > 90%);
"Breathing White " = System in Standby (S3);
Off = System Off (or in Hibernate);

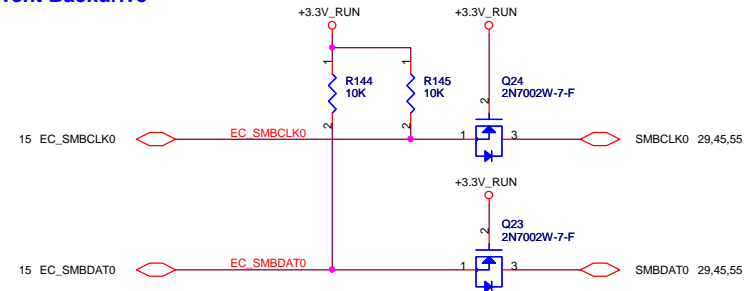
Flashing Amber = Low Battery (S0 and S3 and no AC) when battery charge <10%
Flash rate = on 1/4 sec., off 3/4 sec.



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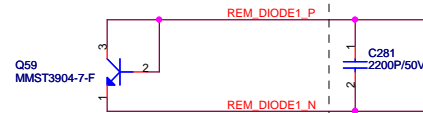


Prevent Backdrive



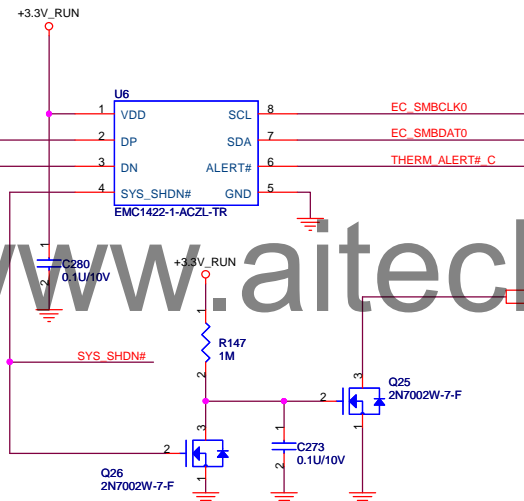
Place these under CPU

10/20mils

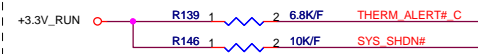


1. Place C579 close to EMC1422
Total capacitance between D+/D- is 2200pF(max)

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OTP 90 degree

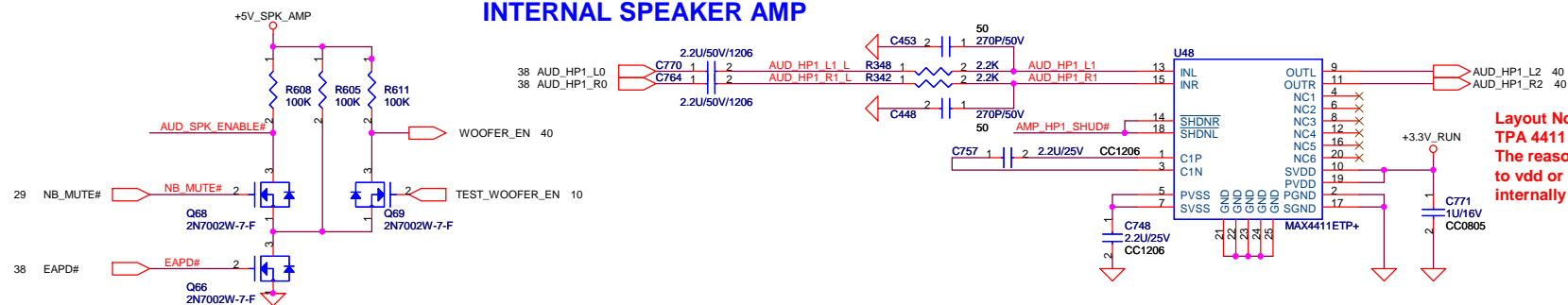


OTP 85 degree : R98 = 10K, R103 = 6.8K
OTP 90 degree : R98 = 6.8K, R103 = 10K

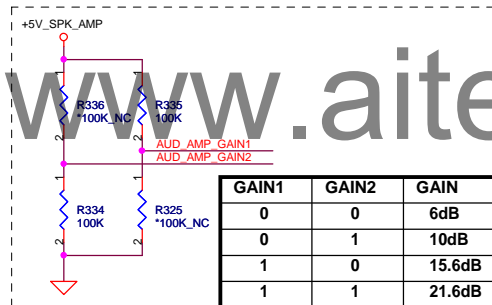
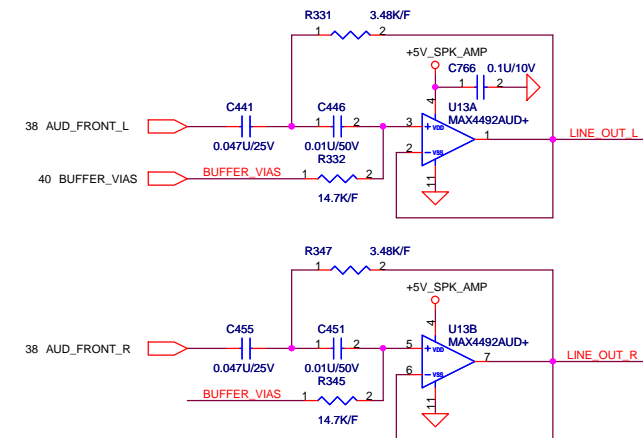
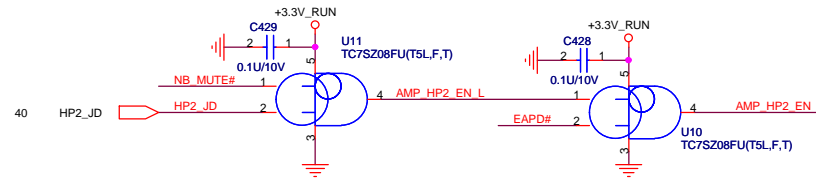
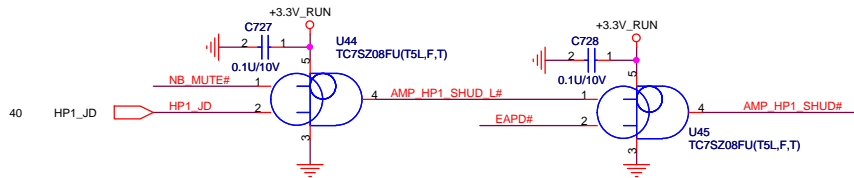


Title			FAN /THERMAL
Size	Document Number	Rev	
	RM5C	C2A	
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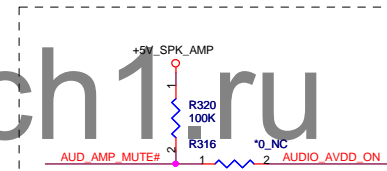
INTERNAL SPEAKER AMP



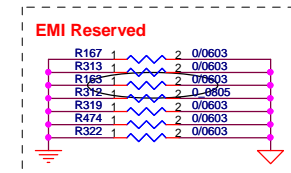
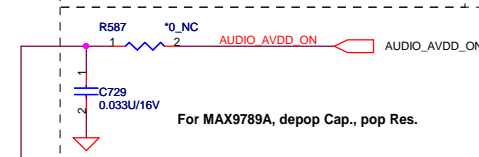
Layout Note:
TPA 4411 : cannot connect EP to GND.
The reason that we can't solder the pad to vdd or ground is because it is internally connected to VSS.



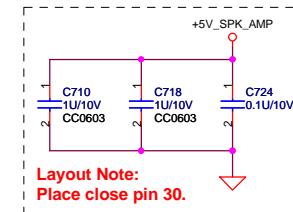
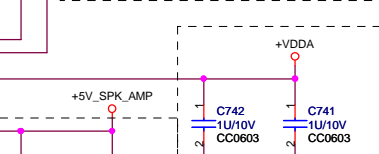
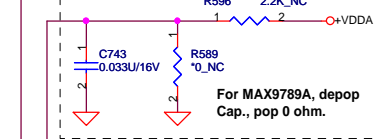
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



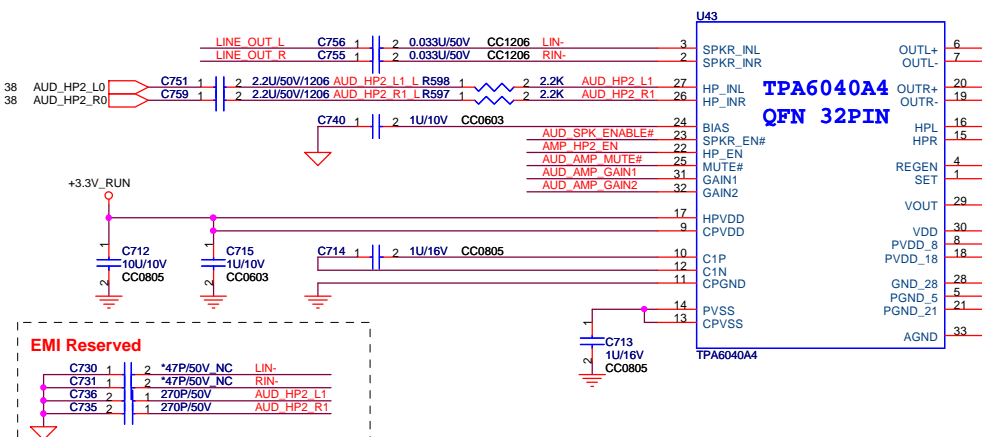
Layout Note:
MAX9789A/TPA6040A : need to connect EP (exposed paddle) to GND.
TPA 4411 : cannot connect EP to GND.
MAX 4411: can connect EP to GND.



7/01: Populate according to EMI request!

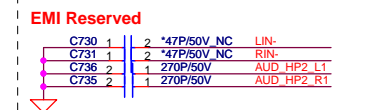


Layout Note:
Place close pin 30.



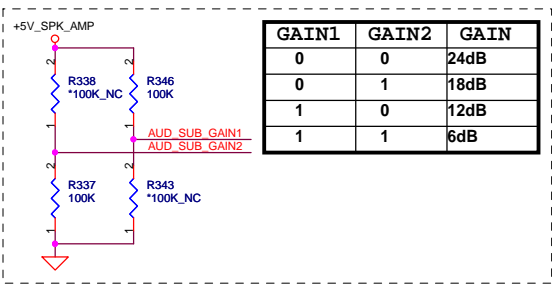
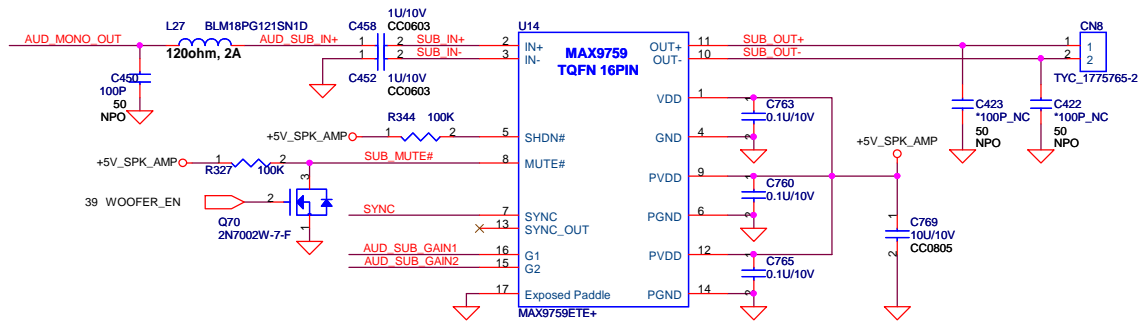
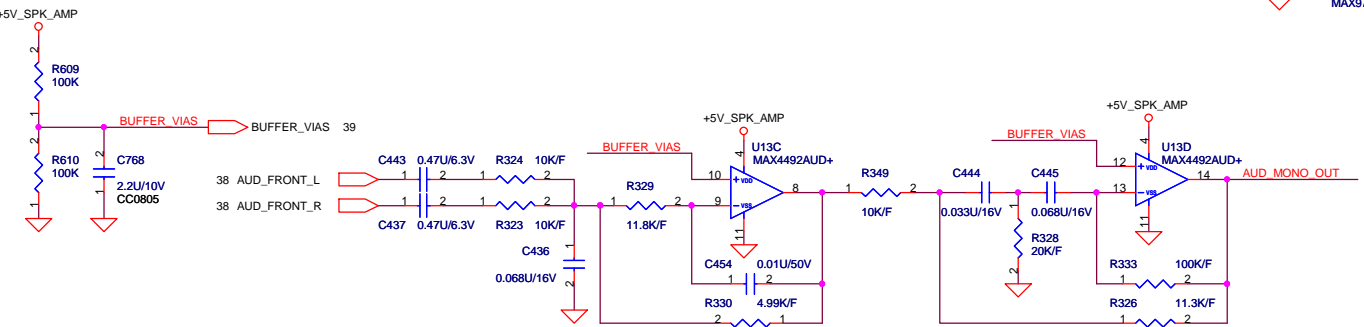
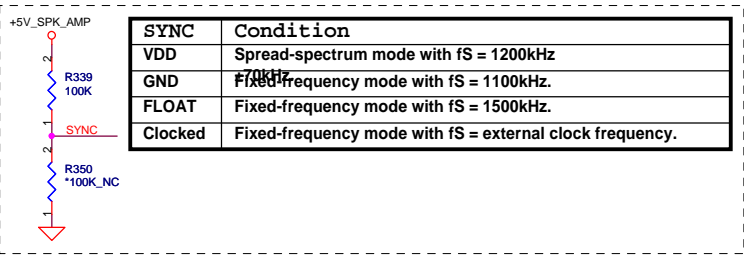
Layout Note:
Place close to pin 18.

Layout Note:
Place close TPA6040.

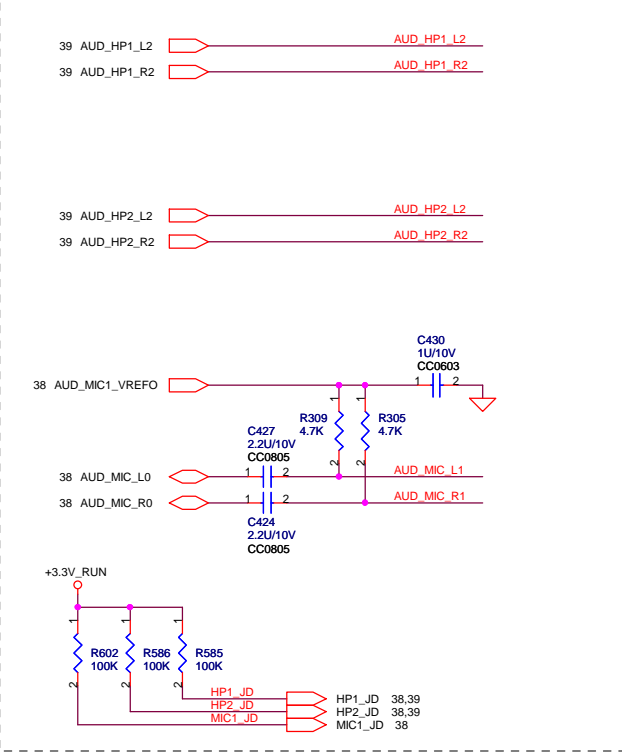


Title			
AUDIO AMP			
Size	Document Number		Rev
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INTERNAL SUBWOOFER AMP

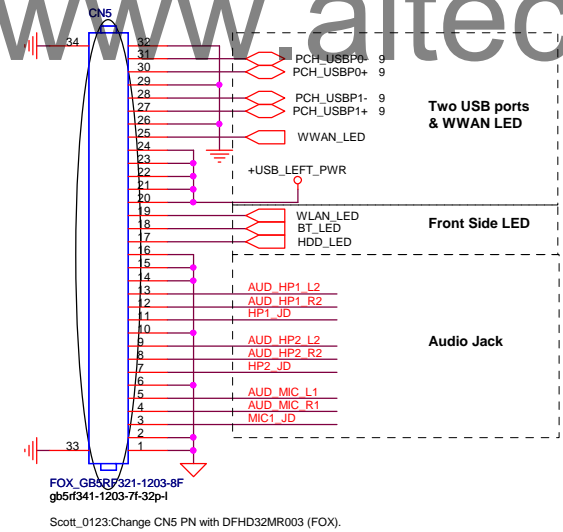


Ambient Parts of Headphone & MIC Jack

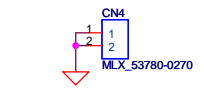


To IB(IO Board) connector

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Adding additional AGND



QUANTA COMPUTER

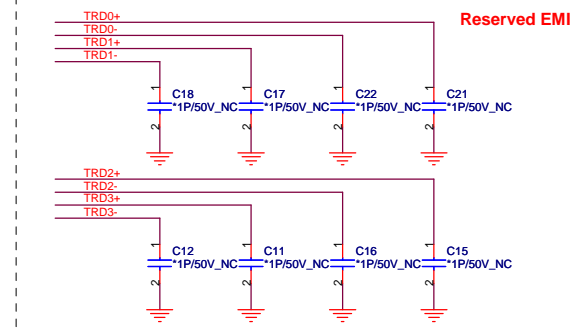
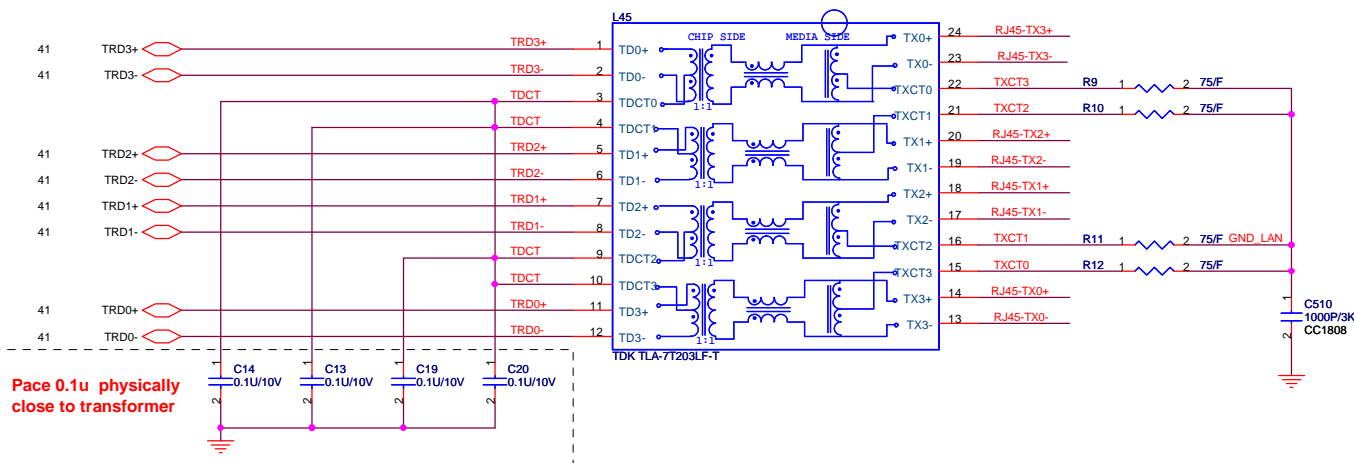
IB CONN & SUBWOOFER

Size Document Number RMSC Rev C2A

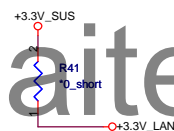
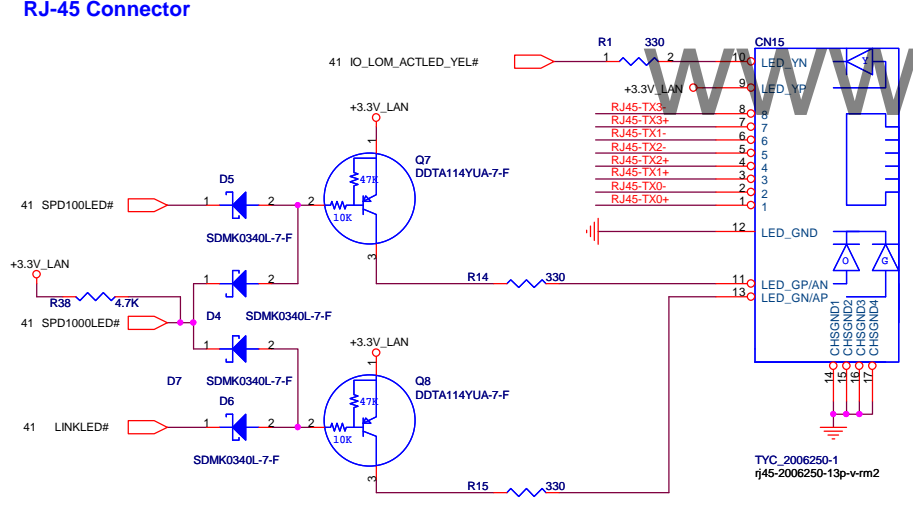
Date: Monday, November 09, 2009 Sheet 40 of 60

TRANSFORMER

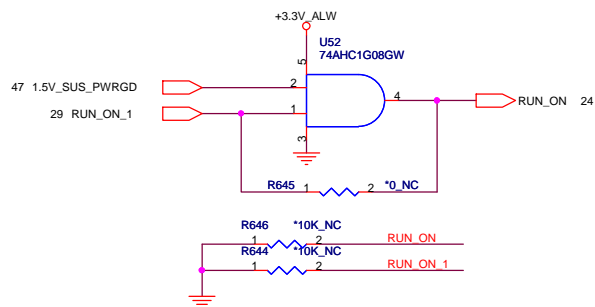
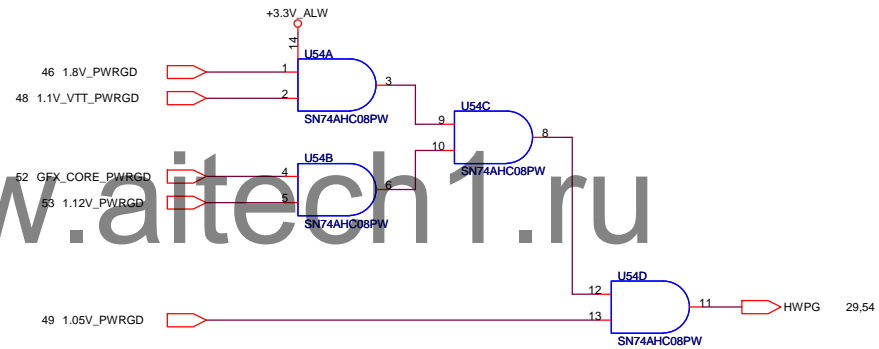
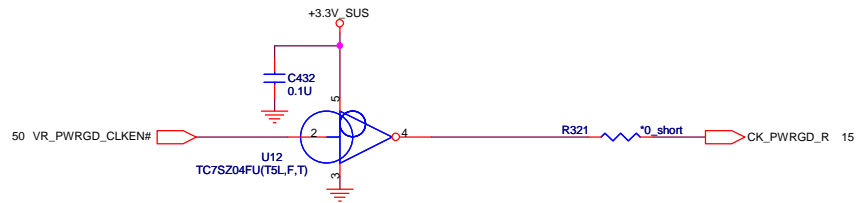
Layout Note:
Route TRD+/- pairs with 100 ohm differential trace impedance.



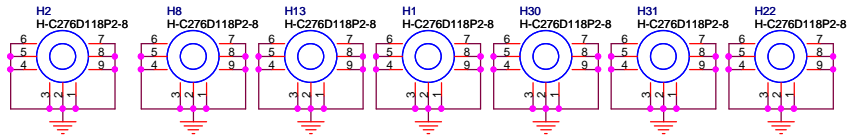
RJ-45 Connector



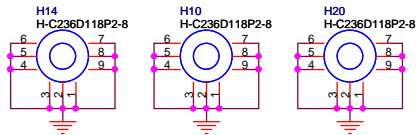
Title			LAN SWITCH
Size	Document Number	Rev	C2A
	RMSC		
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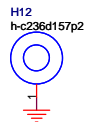
H-C276D118P2-8 * 7



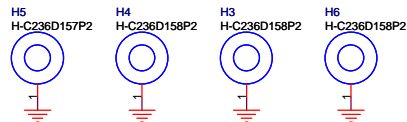
H-C236D118P2-8 * 3



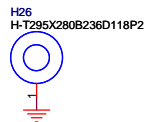
h-c236d197p2 * 1



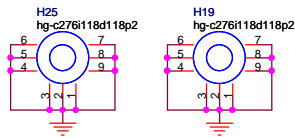
H-C236D158P2 * 4



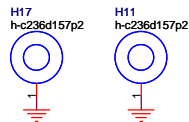
H-T295X280B236D118P2 * 1



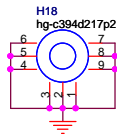
hg-c276i118d118p2 * 2



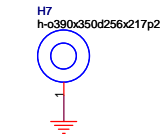
h-c236d157p2 * 2



h-c394d260p2 * 1



H-C394D260P2-8 * 1



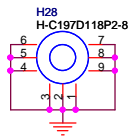
Scott_0731: change H7 & H18 footprint as ME change

Scott_0812:Delete H7 Pin2~Pin9 for layout requite.

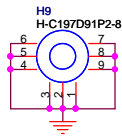
h-c236d236n * 2



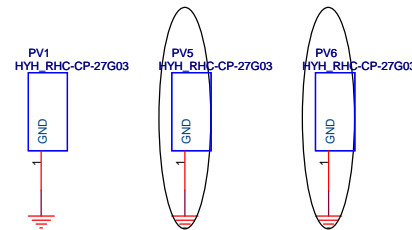
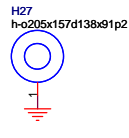
H-C197D118P2-8 * 1



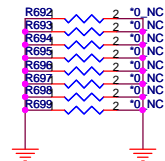
H-C197D91P2-8 * 1



h-o205x157d138x91p2 * 1



Scott_0701:: Added PV6 according to EMI's suggestion

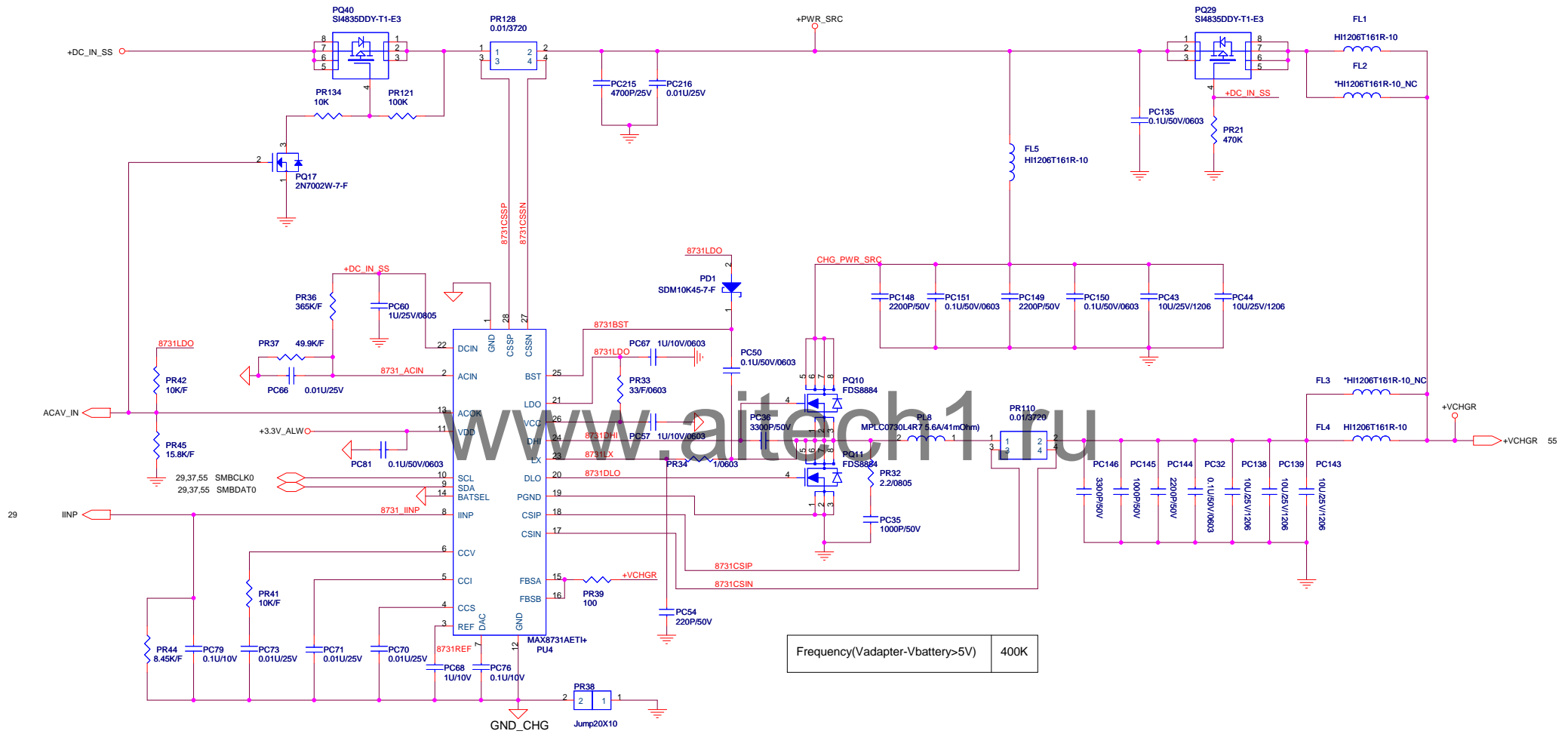


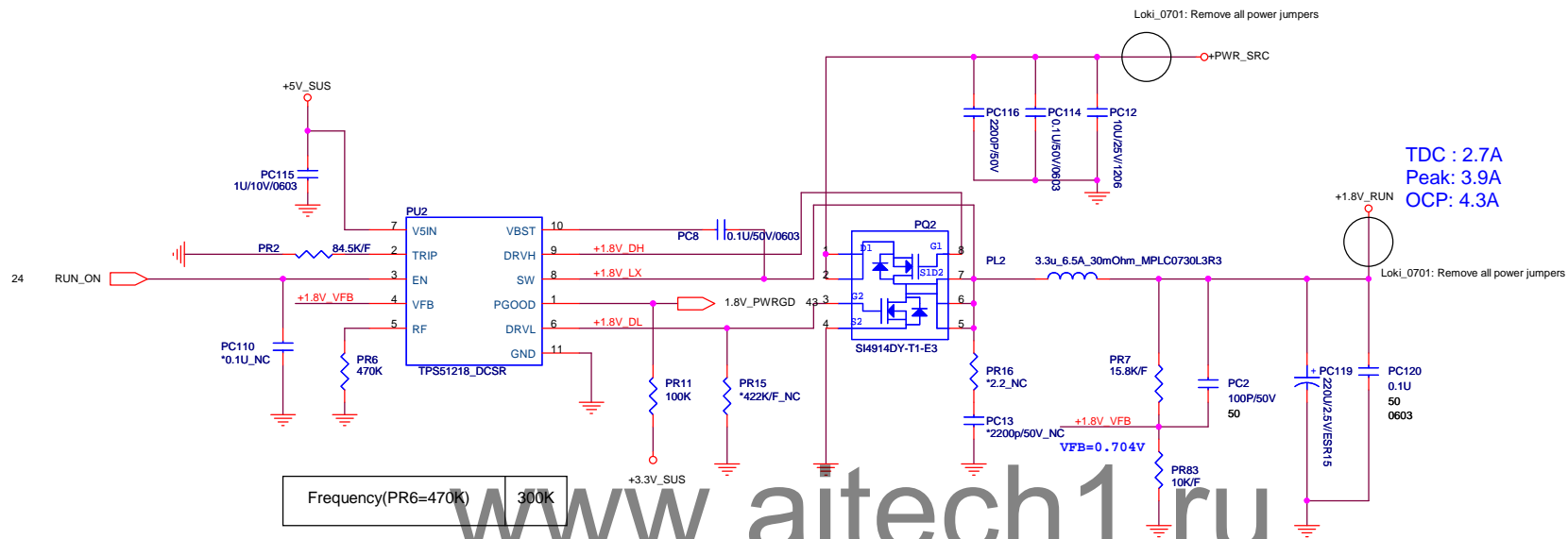
Scott_0703:Add 8pcs 0ohm resistors R692~R699 for thermal issue as EMI concern.

Scott_0707: Reserver R692~R699.

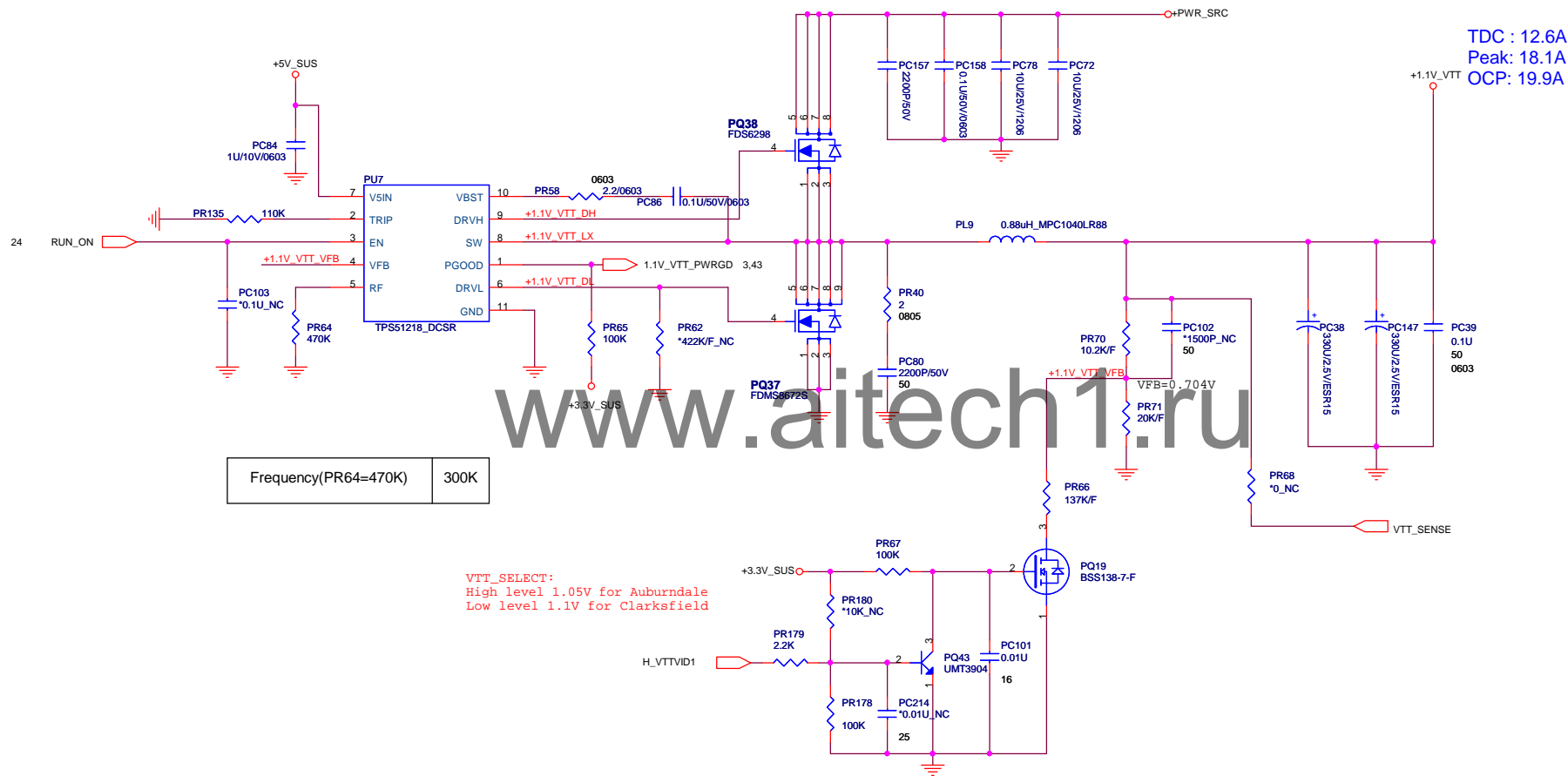


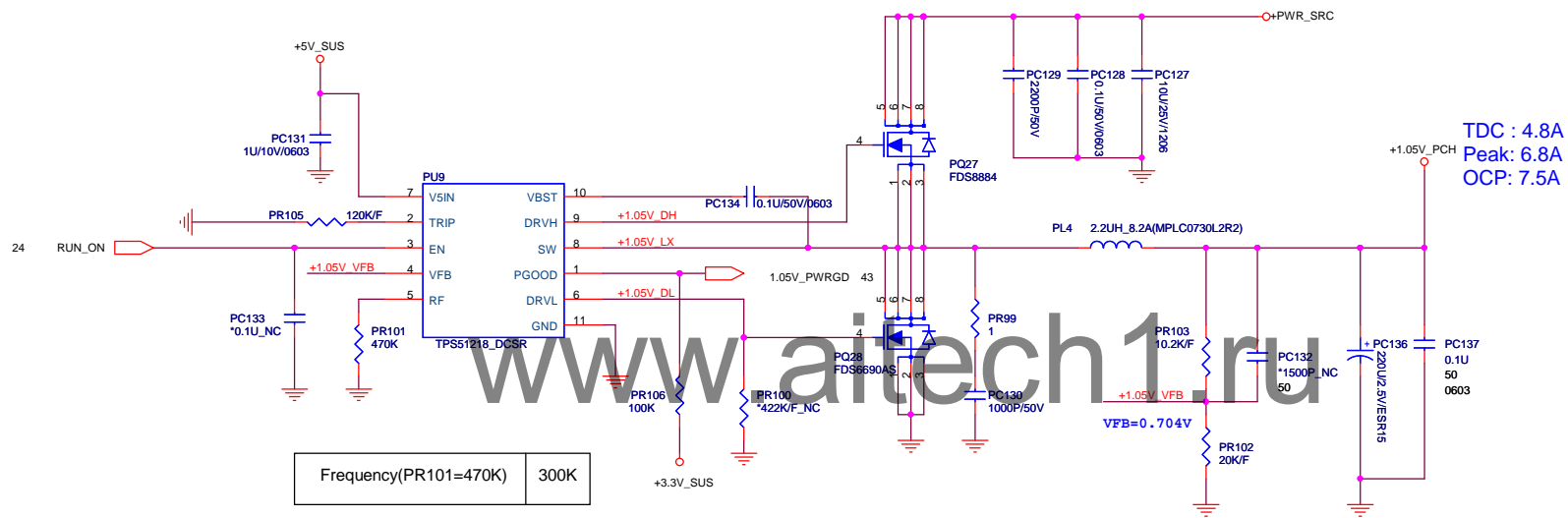
www.aitech1.ru



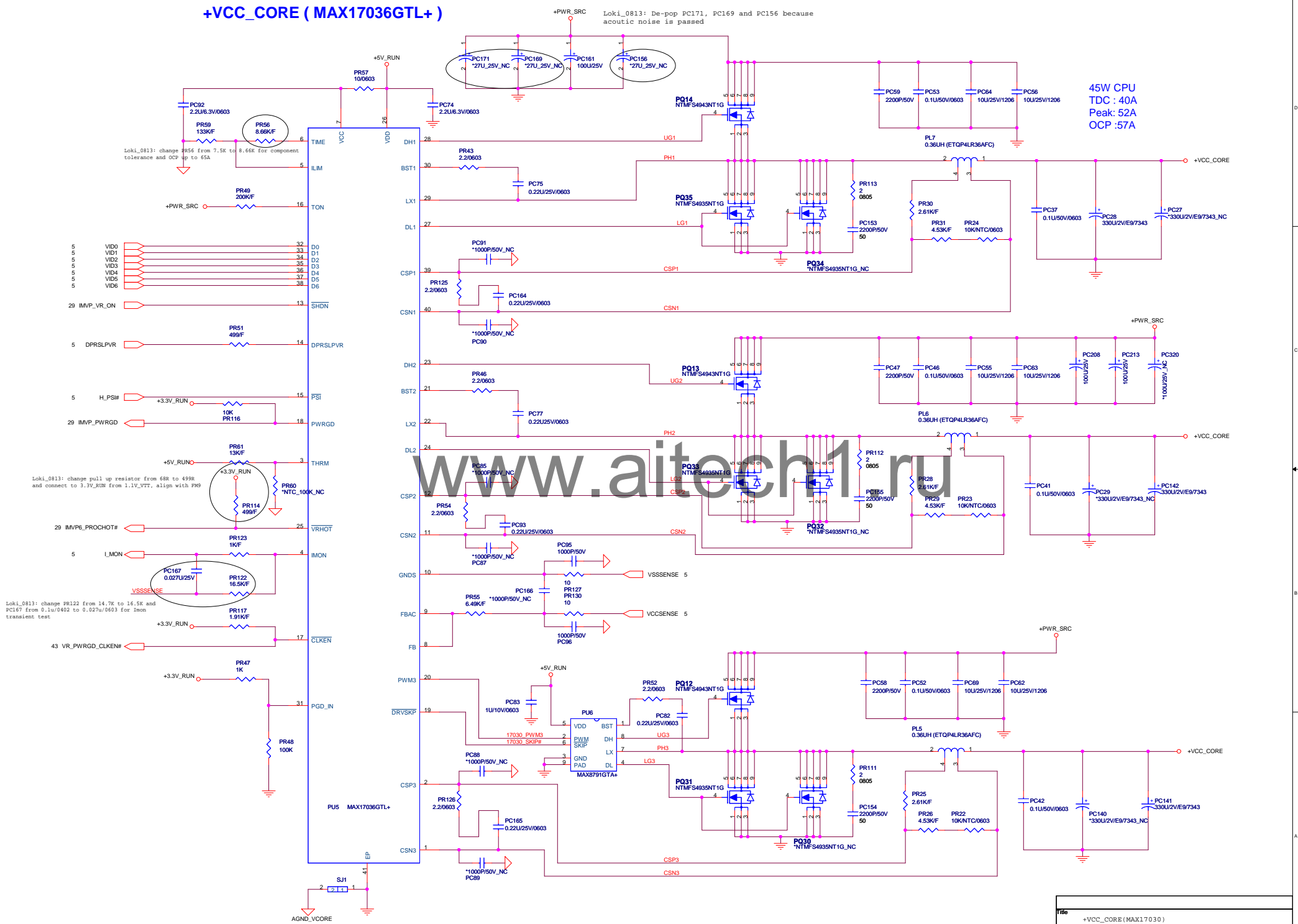


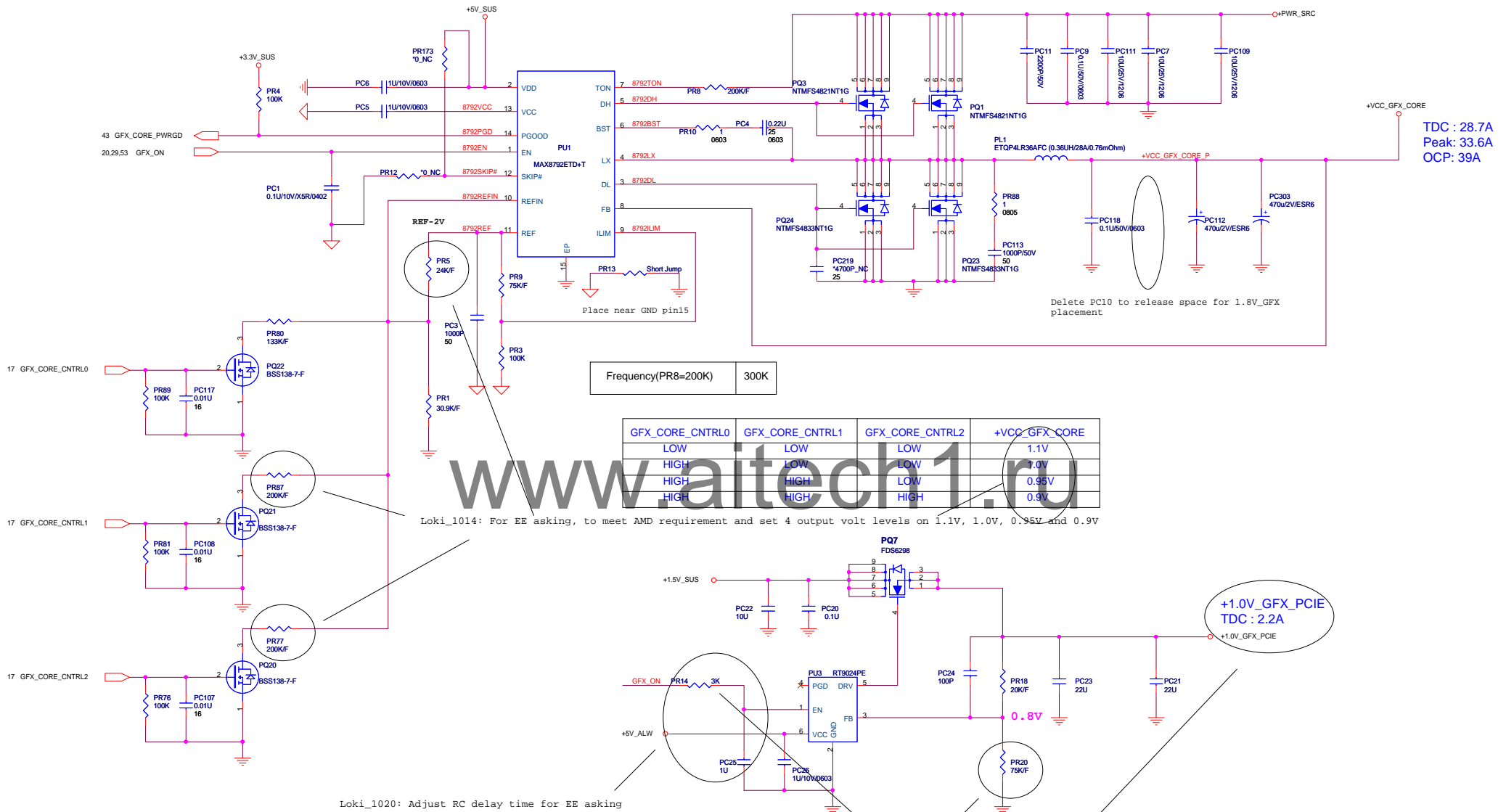
Title		
+1.8V_RUN(TPS51218)		
Size	Document Number	Rev
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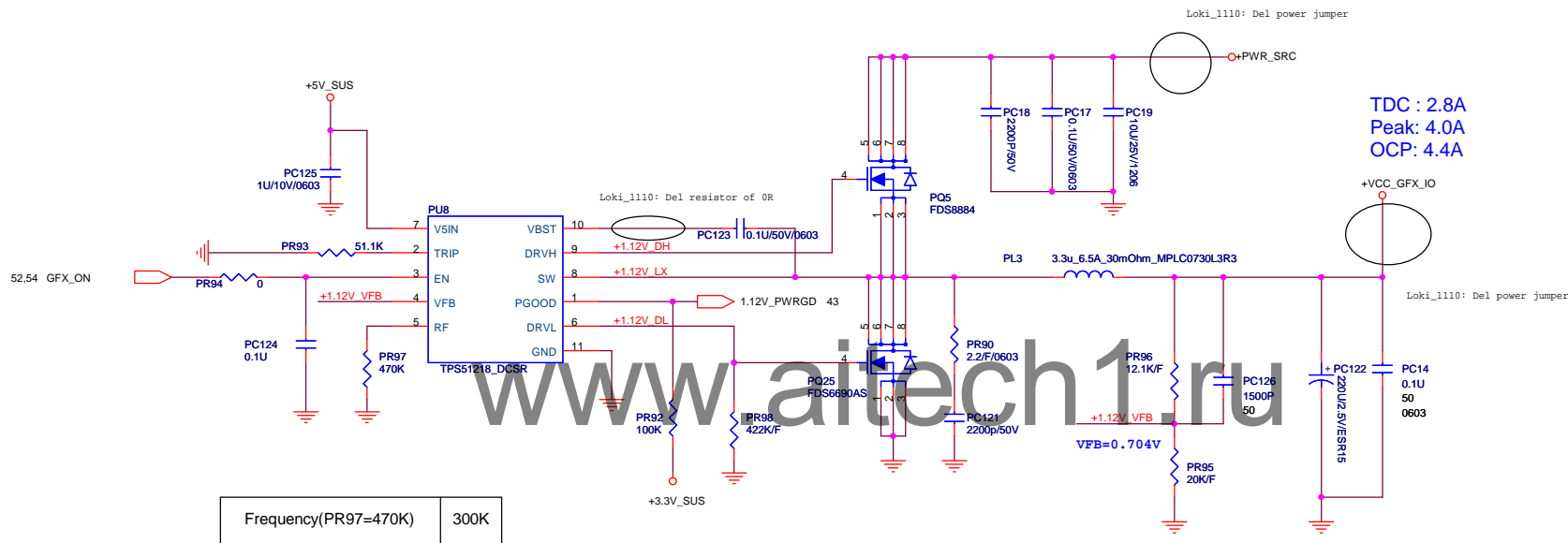




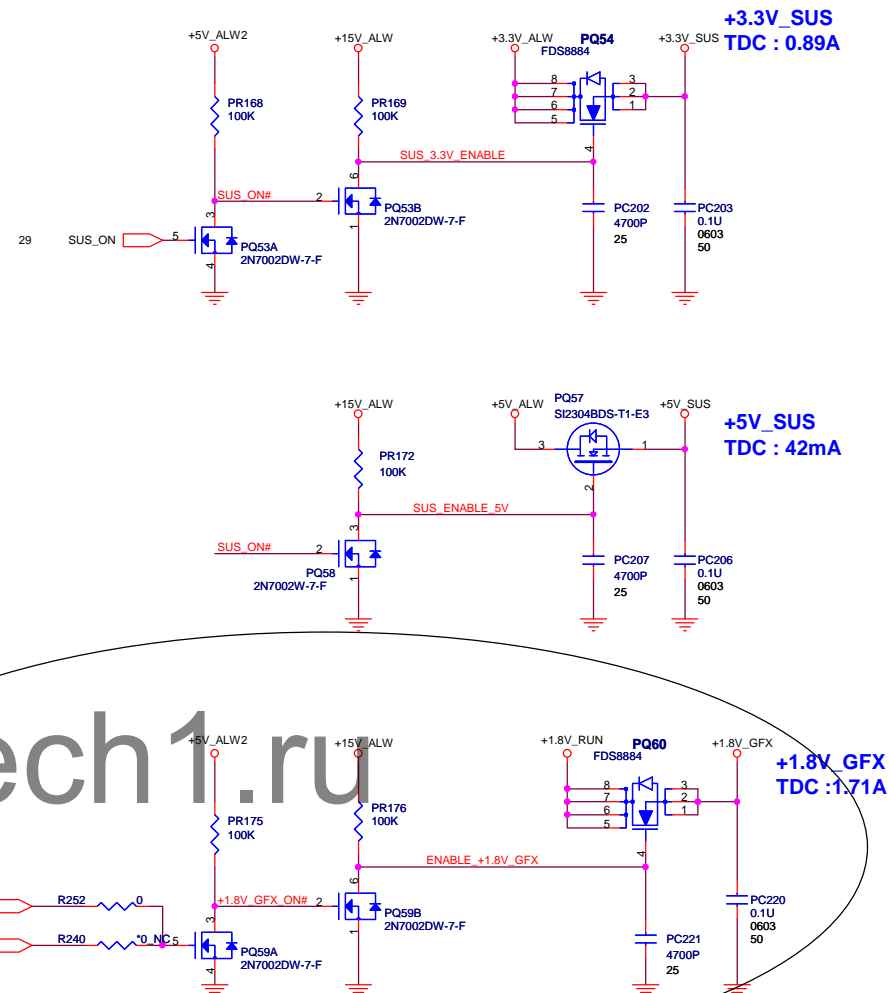
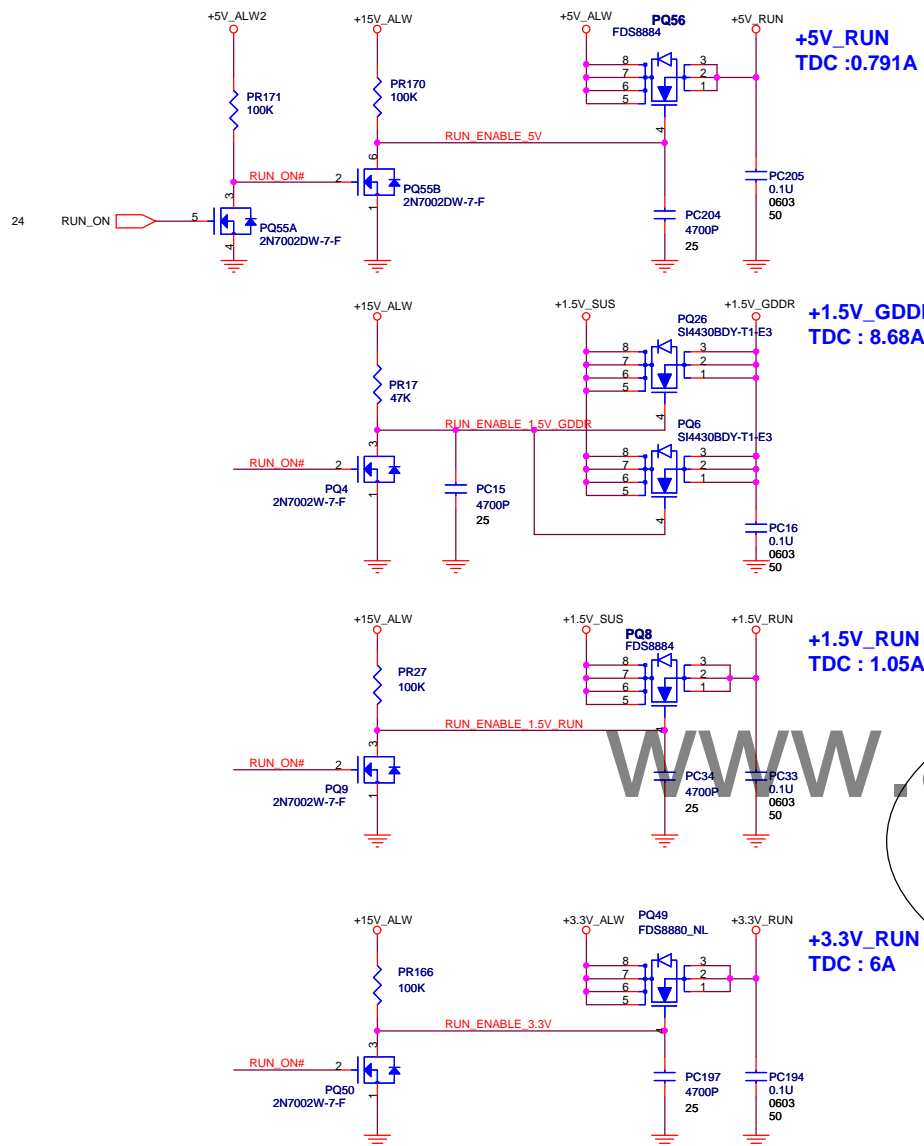
+VCC_CORE (MAX17036GTL+)







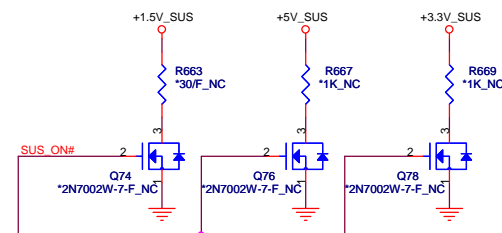
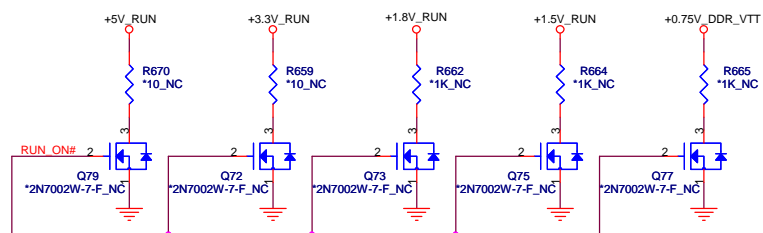
Title		
+VDDCI_M97 (TPS51218)		
Size	Document Number	Rev
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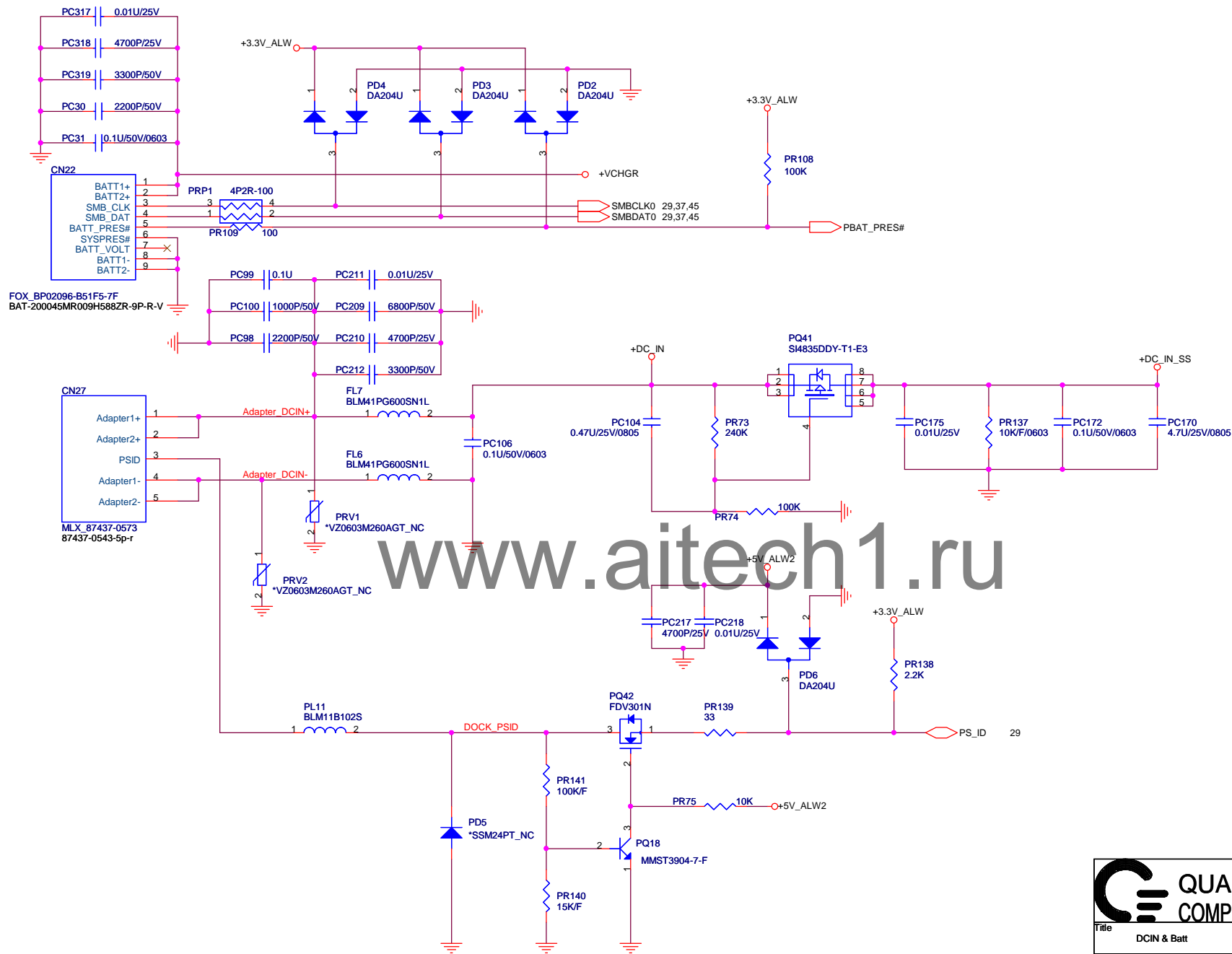
www.aitech1.ru

Loki_1014: For EE asking, to separate +1.8V_RUN and +1.8V_GFX power rail

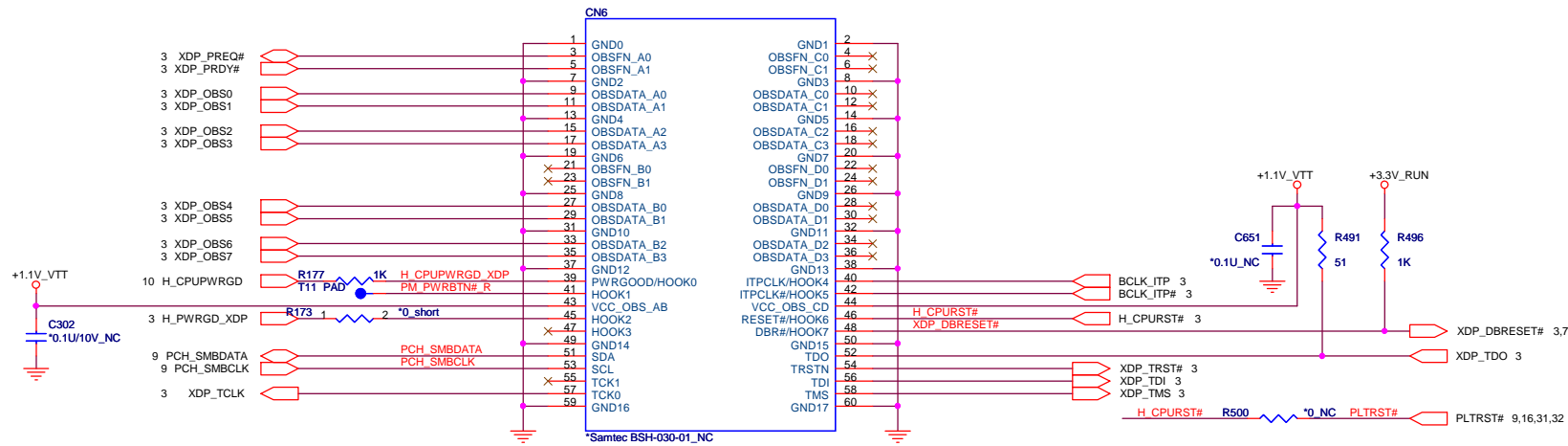
Reserve discharge path



Title: RUN POWER SW		
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CPU XDP

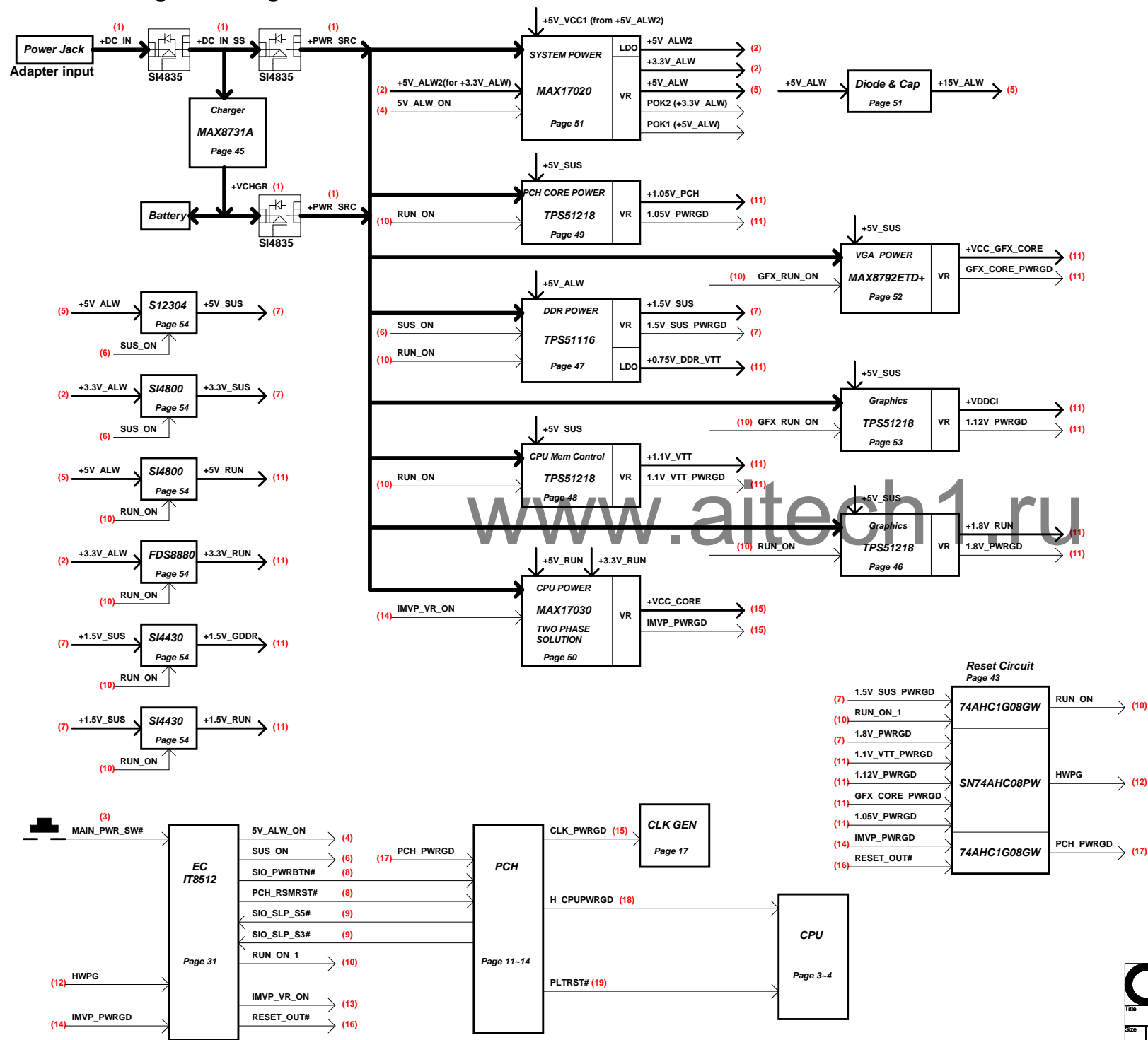


PCH XDP

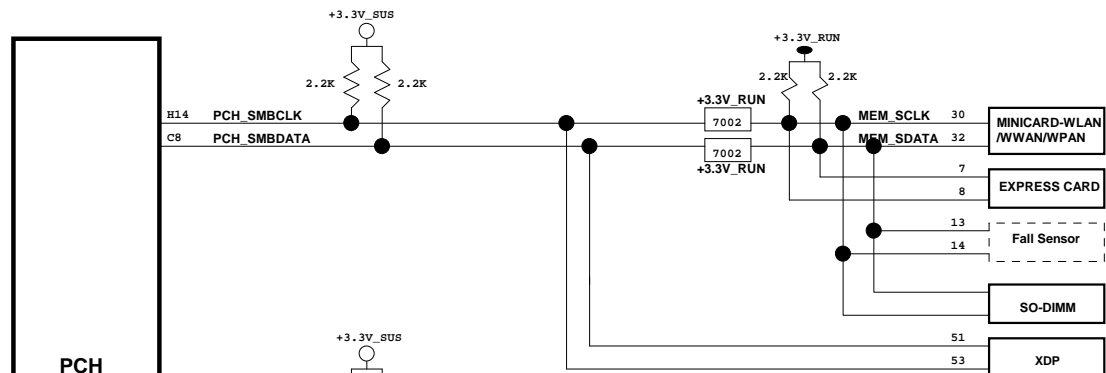
www.aitech1.ru

DEL PCH XDP as FM9 confirmed with Intel that its not necessary!

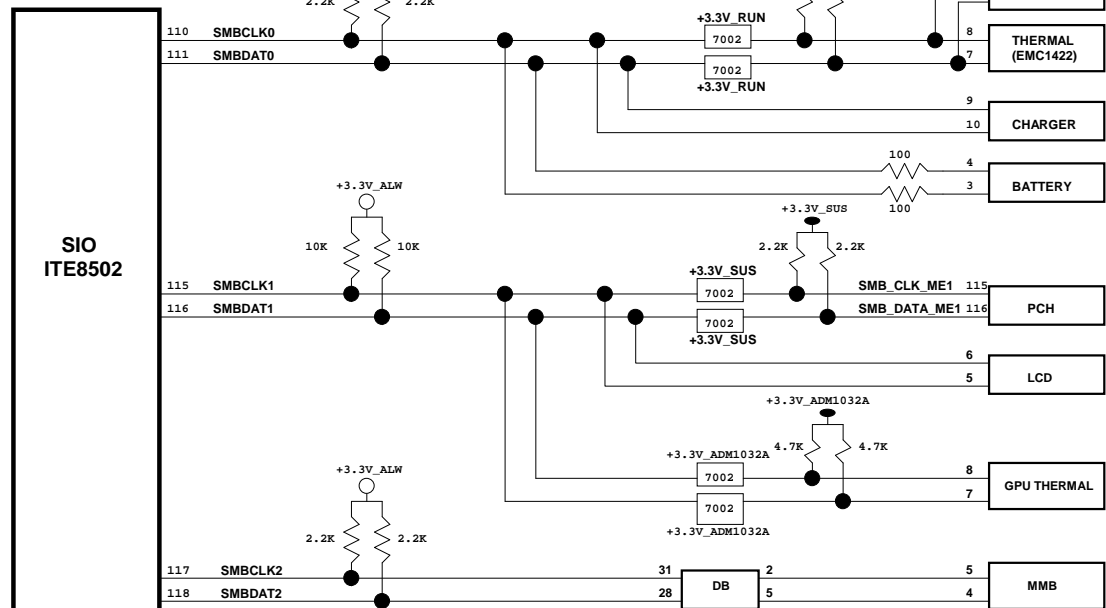
RM5 Power Design Block Diagram 2009/02/25



- (1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
- Bat : +VCHGR -> +PWR_SRC
- (2) +5V_ALW2, +3.3V_ALW
- (3) MAIN_PWR_SW#
- (4) 5V_ALW_ON
- (5) +5V_ALW -> +15V_ALW
- (6) SUS_ON
- (7) All SUS power & PWRGD
- (8) SIO_PWRBTN#, PCH_RSMRST#
- (9) SIO_SLP_S5#, SIO_SLP_S3#
- (10) RUN_ON_1, RUN_ON, GFX_RUN_ON
- (11) All RUN power & PWRGD
- (12) HWPG
- (13) IMVP_VR_ON
- (14) IMVP_PWRGD
- (15) CLK_PWRGD
- (16) RESET_OUT#
- (17) PCH_PWRGD
- (18) H_CPUPWRGD
- (19) PLTRST#



PCH



SIO
ITE8502

POWER STATES

State \ Signal	SLP_ S3#	SLP_ S4#	SLP_ S5#	S4_ STATE#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	N/A	HIGH	N/A	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF	LOW	N/A	HIGH	N/A	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	N/A	HIGH	N/A	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	N/A	LOW	N/A	ON	OFF	OFF	OFF

PM TABLE

power plane \ State	+RTC_CELL	+DC_IN +DC_IN_SS +PWR_SRC +CPU_PWR_SRC +5V_ALW2 +MMB_PWR +3.3V_ALW	+5V_ALW +15V_ALW +5V_SUS +3.3V_SUS +3.3V_LAN +3.3V_CARDAUX +1.8V_SUS +1.5V_SUS	+VCC_CORE +0.75V_DDR_VTT +1.05V_PCH +1.1V_GFX_PCIE +1.2V_LOM +1.5V_RUN +1.5V_CARD +1.8V_RUN +3.3V_RUN +3.3V_DELAY +3.3V_R5C833	+3.3V_RUN_CARD +3.3V_CARD +5V_RUN +LCDVCC +5V_HDD +5V_MOD +5V_SPK_AMP +VDDA +GFX_PWR_SRC
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	OFF	OFF
S5 & S4 with AC or BAT	ON	ON	OFF	OFF	OFF
no AC/Battery	ON	OFF	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
NONE			

PCH IBEX PEAK-M	USB PORT#	DESTINATION
	0	Side pair Top / left
	1	Side pair Bottom / left
	2	USB W/ E-SATA port
	3	Reserved
	4	Mini Card (WLAN)
	5	Mini Card (WWAN)
	6	Reserved
	7	Reserved
	8	Mini Card (WPAN)
	9	TV
	10	Express Card
	11	Camera
PCH IBEX PEAK-M	PCI EXPRESS	DESTINATION
	Lane 1	Mini Card-1 WWAN
	Lane 2	Mini Card-2 WLAN
	Lane 3	Mini Card-3 WPAN
	Lane 4	Express Card
	Lane 5	Cardreader
	Lane 6	LOM